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Fabrication and electrical characteristics of Si nanocrystal/*c*-Si heterojunctions

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Heterojunctions (HJs) were fabricated from *p*-type Si nanocrystals (Si NCs) embedded in a SiC matrix on an *n*-type crystalline Si substrate. Transmission electron microscopy revealed that Si NCs are clearly established, with sizes in the range of 3–5 nm. The HJ diodes showed a good rectification ratio of 1.0×10^4 at ± 1.0 V at 298 K. The ideality factor, junction built-in potential, and open-circuit voltage are ~ 1.24 , 0.72 V, and 0.48 V, respectively. Measurement of temperature-dependent *I*-*V* curves in forward conduction suggests that, in the medium voltage range, junction interface recombination can be described as the dominant current transport mechanism. © 2007 American Institute of Physics. [DOI: 10.1063/1.2787883]

Si nanocrystals (Si NCs) embedded in a dielectric matrix provide a promising material for Si-based optoelectronic devices and third generation photovoltaic (PV) solar cells.^{1,2} By adjusting the Si-NC size, spacing, and barrier height between adjacent Si NCs in the matrix, it is possible to tailor the optical and electronic properties.^{2,3} Si NCs embedded in a Si oxide or nitride have been widely investigated,^{4,5} but Si NCs in a SiC matrix (Si-NC:SiC) have not received as much attention. They are of particular interest because the reduced barrier height between adjacent Si NCs is conducive to carrier transport.⁶ Recently, it has been demonstrated that Si-NC:SiC material can be made by high temperature annealing of Si-rich amorphous $\text{Si}_{1-x}\text{C}_x$ produced by magnetron sputtering⁷ or plasma-enhanced chemical vapor deposition.⁸ In this letter, we present results on fabrication and electrical characterization of *p*-type Si-NC:SiC/*n*-type crystalline Si (*c*-Si) heterojunctions (HJs) deposited by magnetron sputtering. The study of the Si-NC:SiC/*c*-Si HJs is not only important for evaluating the electrical material quality of the Si-NC:SiC films toward their use in PV solar cells, it also offers insight into the electrical properties for this kind of HJs, which are of considerable interest as wide-band gap emitters or window regions in bipolar transistors⁹ and photodetectors.¹⁰

Si-NC:SiC/*c*-Si HJs were fabricated on *n*-type Si wafers, (100) oriented with a resistivity of 2–9 $\Omega\text{ cm}$, corresponding to a doping density of $(0.4\text{--}2.5) \times 10^{15}\text{ cm}^{-3}$. In addition, quartz substrates were used for optical measurements. The amorphous $\text{Si}_{1-x}\text{C}_x$ /SiC ($x \sim 0.1\text{--}0.15$) multilayers were deposited by magnetron cosputtering from Si and SiC targets using a computer-controlled AJA ATC-2200 system. The SiC target was boron doped, with the intention that boron would be incorporated in the multilayer films. The thickness of individual layers was typically ~ 6 nm ($\text{Si}_{1-x}\text{C}_x$) and ~ 2.5 nm (SiC) and the total emitter thickness was about 160 nm. The use of the $\text{Si}_{1-x}\text{C}_x$ /SiC multilayer instead of a single $\text{Si}_{1-x}\text{C}_x$ layer is expected to give better control of Si-NC size, as the Si-NC size is constrained by the thickness of the Si-rich layer.^{3,4} The samples were not intentionally

heated during the deposition process. The as-deposited samples were annealed at 1100 °C for 9 min in a conventional furnace in N_2 atmosphere, with Si NCs precipitating from the Si-rich material. A back Ohmic contact covering the full area of the rear surface was fabricated by vacuum evaporation of Ti (~ 30 nm) followed by Al ($\sim 1.0\text{ }\mu\text{m}$). The front electrode consists of an Al metal grid so as to allow illumination, which was formed by evaporating Al through a silicon shadow mask. The final device area is $1.0 \times 1.0\text{ cm}^2$, which was defined by laser scribing.

Figure 1 shows a typical cross-sectional transmission electron microscopy (TEM) image of an as-deposited Si-NC:SiC/*c*-Si HJ diode. The inset shows the formation of Si NCs after annealing at 1100 °C. The as-deposited sample indicates two uniform amorphous phases within a clear layered structure. After annealing, we can clearly see lattice fringes in a material surrounded by an amorphous matrix, indicating the formation of the NCs. The spacing of these lattice fringes corresponds to Si {111} lattice planes. The Si-NC size obtained from TEM images is in the range of 3–5 nm. The formation of Si NCs in the annealed samples was also confirmed by Raman spectroscopy and x-ray diffraction (XRD) measurements.⁷ XRD showed the formation

FIG. 1. Typical cross-sectional TEM image of an as-deposited Si-NC:SiC/*c*-Si HJ diode. The inset shows the formation of Si NCs after annealing at 1100 °C for 9 min.

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FIG. 2. (Color online) Dark I - V curves of a typical (p) Si-NC:SiC/ (n) c -Si HJ diode: (a) the semilogarithmic and the log-log plots at 298 K in both polarities, and (b) the forward I - V - T curves measured from 298 to 368 K in 10 K steps. The symbols are measured data and the dashed lines in the plot of (b) are fits of the curves in region II. The inset in the plot (b) shows the diode ideality factor n and a modified Arrhenius plot of the J_0 as a function of $1/T$.

of Si NCs accompanied by the presence of nanocrystalline β -SiC. The fraction of β -SiC depends on the sample stoichiometry. The optical band gap $E_{g\text{opt}}$ was extracted from a Tauc plot. The $E_{g\text{opt}}$ increases from ~ 1.4 eV (as deposited) up to ~ 2.0 eV (annealed at 1100 °C).¹¹

Figure 2 shows the dark current-voltage (I - V) characteristics of a (p) Si-NC:SiC/ (n) c -Si HJ diode: (a) the log-log plot (the inset is a semilogarithmic plot) at 298 K in both polarities and (b) the forward temperature-dependent I - V (I - V - T) curves measured from 298 to 368 K in 10 K steps. The diode shows a good rectification ratio of 1.0×10^4 at ± 1.0 V at 298 K. Three distinctly different regions (labeled I, II, and III) can be identified in the log-log plot and I - V - T curves. At low voltages (region I, $V < 0.1$ V), it was found that the forward and reverse currents are nearly the same [see Fig. 2(a)], and the relationship between $\log I$ vs $\log V$ gives a slope of ~ 1 , indicating that the presence of a parallel current path due to an Ohmic shunt resistance R_{sh} in parallel to the

junction is responsible for these currents.¹² The diode current is given by Ohm's law $I = V/R_{\text{sh}}$ ($R_{\text{sh}} = 1.90 \times 10^5 \Omega \text{ cm}^2$).

At intermediate voltages (region II, $V \sim 0.1$ – 0.4 V), the temperature dependence of the saturation current density J_0 and the pre-exponential term A were extracted by fitting the I - V curves using a diode equation $J(V, T) = J_0(T) \exp(AV)$ [see Fig. 2(b)]. In general, there are two models for explaining the current transport mechanisms through a junction: (i) A is temperature dependent (specifically, $A = q/nkT$, where q is the electron charge, T is the temperature, k is the Boltzmann constant, n is ideality factor, and $n = 1.0$ for a diffusion-limited model and $n \leq 2.0$ for a recombination-limited model), and (ii) $A = \text{constant}$ for a tunneling-limited model. It is found that the A has a linear dependence with $1/kT$ and decreases with an increasing temperature, which rules out the tunneling mechanisms across the junction. From the temperature dependence of $A = q/nkT$, n values of ~ 1.24 were obtained at temperatures ranging from 298 to 368 K. The extracted n value, together with the temperature dependency of A , indicates that the recombination process is the most probable current flow mechanism in region II. An activation energy E_a was calculated by a modified Arrhenius plot [see the inset in Fig. 2(b)] using the equation $J_0 = J_{00} \exp(-E_a/nkT)$ to identify different recombination mechanisms,¹³ where J_{00} is a weakly temperature-dependent prefactor. In the case of neutral bulk and space charge region recombination, E_a represents the band gap energy E_g of the absorber material ($E_g = 1.12$ eV for Si); whereas for interface recombination, E_a represents the effective barrier height ϕ_B for charge carriers from the absorber Si to recombine at the interface. We obtained $E_a = 0.83$ eV from the slope of the plot, which is close to $\phi_B = 0.96$ eV from C - V measurements ($\phi_B = V_{\text{bi}} + E_F^n$, where V_{bi} and E_F^n are the built-in potential and bulk Fermi level in Si substrate, respectively; see later discussions). It suggests that the recombination mainly takes place at the junction interface.

At large voltages (region III, $V > 0.4$ V), the slopes of the I - V curves are reduced and deviate from exponential behavior. From a $\log I$ - $\log V$ plot, for a bias voltage up to 3 V, the I - V characteristics show a power-law dependence. This suggests that currents were limited by a space-charge limited current (SCLC) conduction described by $I = KV^M$,¹⁴ where M depends on the density of states in the Si-NC:SiC layer and K is a function of film thickness and trap distribution. It is found that the M value varies from 1.5 to 1.1 in the measured temperature range and increases with decreasing temperature. It should be noted that the SCLC electron transport has also been demonstrated in Si-NC films by investigating macroscopic electronic conduction across films.^{14,15}

Figure 3 shows capacitance-voltage (C - V) characteristics measured at a frequency of 100 kHz. The $1/C^2$ - V plot reveals a good linear relationship in a wide voltage range from -5 to 0.1 V, indicating that the abrupt junction theory is applicable to the devices.¹⁶ The $1/C^2$ - V intercept of 0.72 V is equal to the built-in potential V_{bi} of the device within the Si substrate when neglecting the influence of interface states on the capacitance. The slope of the curve gives a substrate doping concentration of $2.2 \times 10^{15} \text{ cm}^{-3}$, which agrees well with the resistivity of the n -Si substrate used in these devices. The bulk Fermi level E_F^n in the Si substrate was calculated by this doped density to be $E_F^n = 0.24$ eV below the Si conduction band edge.

FIG. 3. (Color online) $1/C^2$ vs voltage plot of a typical (p) Si-NC:SiC/(n) c-Si HJ diode. The squares are measured data and the solid line is the extrapolation to the voltage axis.

The device photovoltaic properties were evaluated by the quasi-steady-state open-circuit voltage (suns- V_{oc}) method.¹⁷ Figure 4 shows that the 1-sun V_{oc} is 480 mV. The measured curve is fitted with a two-diode model with fixed ideality factors of $n=1$ and $n=2$ and a shunt resistance. Generally, the $n=2$ diode accounts for recombination in the junction space charge region, whereas the $n=1$ diode accounts for bulk and surface/interface recombination.¹⁷ It can be seen that the two-diode model describes the measured diode characteristics well throughout the entire injection range and the fitted curve has $n \sim 1.2$ for $V_{oc}=0.4-0.5$ V, consistent with the n value of the dark I - V curves at intermediate bias voltages. The parameter V_x (~ 0.4 V), where the $n=1$ and $n=2$ curves cross each other, is the point at which the dominant region for each diode changes. For voltages below V_x , $n=2$ recombination is dominant, whereas for higher voltages, $n=1$ recombination dominates the illuminated I - V curve. The

FIG. 4. (Color online) Measured suns- V_{oc} characteristics of a (p) Si-NC:SiC/(n) c-Si HJ diode. The solid lines are the fitted curve using a two-diode model. The dotted line is calculated from a diode equation with $n=1.2$ as a guide to the eye. The shunt resistance is so large as to not have an effect in the investigated light intensity range.

V_x is lower than V_{oc} in this device and thus 1-sun V_{oc} is predominantly limited by $n=1$ recombination, caused mainly by defects at the junction interface due to a large difference in the thermal expansion coefficient of Si and SiC ($\sim 8\%$) during annealing.

In conclusion, we have fabricated p -type Si-NC:SiC/ n -type c -Si HJs by magnetron cosputtering followed by a postdeposition anneal. TEM investigations show evidence of Si NCs embedded in a SiC matrix. The diode has a good rectification ratio of 1.0×10^4 at ± 1.0 V at 298 K. The n , V_{bi} , and V_{oc} are ~ 1.24 , 0.72 V, and 0.48 V, respectively. The I - V - T results suggest three different carrier transport mechanisms in forward conduction. At intermediate bias voltages, junction interface recombination is the main transport mechanism.

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