

Fabrication of cracking-free CeO₂ thin film using UV/O₃ and plasma treatment and their applications in wearable devices

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Fabrication of Cracking-free CeO₂ Thin Film Using UV/O₃ and Plasma Treatment and their Applications in Wearable Devices

Yiting Qin

**A thesis in fulfilment of the requirements for the degree of
Master of Engineering**



Supervisor: Dr. Dewei Chu

School of Materials Science & Engineering
Faculty of Science

March 2019

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ABSTRACT

Recent development of wearable devices in healthcare, wearable and soft robotics has generated increasing demand for memory devices which are more compact with higher data storage capacity and mechanical flexibility, as well as lower fabrication costs. Resistive random access memory (RRAM), which is an emerging technology, has unique advantage of high response speed, low power consumption, and 3D stack architecture.

In this research, a sandwich structure (Au/CeO₂/Au/Si) based RRAM device has been developed. Scanning electron microscope (SEM), transmission electron microscopy (TEM) were applied to analyze the phase and microstructure for both inks and the thin films. The electrical properties including current-voltage (I-V) response were systematically tested by auto-lab and source meter. A stretching test also was done with a thermoplastic polyurethane (TPU) based device.

A suspension ink with controlled shape of CeO₂ nanocrystals was prepared. A series of samples have been prepared with solvent, toluene or hexane, by using CeO₂ as core material for the ink. The thin film was deposited by spin coating or drop-coating following with plasma treatment. Both silicon and TPU based device have been used as substrates for comparison.

Shape controlled CeO₂ nanocrystals and printable inks have been successfully fabricated. Different solvent was used to vary the properties of the ink and improve the cracking-free films. A large area cracking-free CeO₂ thin film was

obtained by plasma processing. Ink jet printing method was also involved as one method of film fabrication. The memory behaviour could be more clearly demonstrated with obvious characteristic from the I-V curve both at silicon and TPU elastic substrates. Thus, the plasma treatment with different treatment time and power could help improve the thin film performance. A simple flexible device had been manufactured with a basic memory behaviour.

In summary, the project provided a systematic study on developing metal oxide based nanocrystals towards crack-free thin film and memory devices applications, which may have potential applications in future printed, flexible data storage devices.

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1. INTRODUCTION

Information technology has been developed in an incredible high speed during the last decade. 'Evolution' of computing devices aims to achieve more accuracy with higher speed and smaller volume. Moore's diagram [1], cost versus integration density, introduce a rule that the more transistors integrated, the lower cost for each transistor. This can be only down to a certain minimum, after that, the cost climbed steeply. Currently, the silicon-based semiconductor has been taking great strides along this diagram which remains to improve the speed, cost and size for manufacturing. The conventional memory devices based on transistor are predicted to approach the scaling limit in 2018 [1]. More wearable applications [2] are developed to support and create an integral part of people's normal life and users who wear it can always access them no matter what place or time. Hence, one of the most prominent challenges today is to make a combined device with both small size and large capacity in memory technology. The wearable properties can be implemented in resistive switching devices [3]. The experiment in this thesis was focused on the research of achieving the wearable function by using the self-assembled [4] ink to fabricate the transition-metal-oxide-based [5] device with its electrical properties.

A simple model device has the structure of metal oxide thin film in between of top and bottom electrode. Cerium(IV) oxides, CeO_2 or ceria [6], were used as resistive switching materials. The gold (Au) coating monocrystalline silicon chip and pure gold [7,8] were used as bottom and top electrode, respectively. A hydrothermal process [9-11] was used to produce inks, which is shape-controlled in the autoclave by engineering the liquid-liquid Interface [9]. A

simple drop-coating method was introduced following by plasma or UV treatments to fabricate the CeO_2 thin film. This method with cost effectively and rapid production was an effective way that can be taken under mild temperatures. Several controlling parameters for this method, such as shape of the precursor, solvents of the ink, treatment time and etc. have been tested. Unique properties of the ink would be produced under different conditions. As a result, the different microstructure of the thin films and distinct influence for properties of the memory application were shown by the current-voltage (I-V) curve. SEM and TEM microscope were used as reference in studying the microstructure and composition.

Cubic shaped nanocrystals of CeO_2 were obtained by adding oleic acid [12] during the hydrothermal process. Different self-assembly percentage of the ink has been achieved. Interesting resistive switching [3] phenomenon was observed in the device. The device with high-resistance state was be switched into a low-resistance state after applying an external electrical field. This phenomenon was reversible by subjecting to an opposite voltage. Thus, the device could remember the last resistance it has during this process. A 'pinched-hysteresis loop' [13] showed on a resistance graph could demonstrate this property. Therefore, it could be seen as a footprint of memristive devices.

The aim of this thesis is to (1) seek for methods of synthetic process of self-assembled CeO_2 printable ink; (2) analyze the data obtained and find out the suitable conditions for fabricating the CeO_2 thin film and (3) to determine the properties of the thin film especially with the desired electrical properties to realize the memristive function.

2. LITERATURE REVIEW

2.1 Background

2.1.1 Wearable Devices

The 21st century, also called Information Age [14], has many upsides. People rely on the new technologies due to the rapid innovation of robots, electronic circuits, sensors, artificial synapses and etc. [15]. Meanwhile one of the major downsides caused by this high speed evolution is that information overladed[2]. The huge amount of information will easily push the limitation of the storage as people can imaging. Three Mile Island Accident [16], Chernobyl Disaster [17], and more closely Fukushima Nuclear Power Plant Disaster [18] are three results caused by overladed of the information. Similarly, this pressure has applied to human's normal life. Computers has successfully shrunk from room size (Atanasoff–Berry Computer [19], contained 280 dual-triode vacuum tubes , 31 thyratrons, a wire of approximately 1.6 km in length, and was about a size of a desk, weighed more than 320 kg [20]) to palm size (cell phone, iPad, laptops) enable the practical requirement for user's lifestyle.

A simple structure of a wearable device contains a backpack PC, a head-mounted display, input devices and a wireless communication hardware. To define a device as a wearable device, it should meet three goals: mobility, augment reality and context sensitivity. The wearable device can go with the wearer and be aware of the user's surroundings. The wearable devices with operational and interactional constancy can be distinguished from other traditional forms of large size portable computers.

2.1.2 Transparent Flexible Electronics

Two important characteristics for developing the next-generation wearable device are transparency and flexibility for the electronic circuitry. Moore's Law has led the manufacturing of silicon-based semiconductor nearly 50 years, which predicted an accurate capacity of transistor with lowest cost. This rule is estimated to reach its end of scaling, a linewidth of 12nm, in 2018 owing to the heat produced during operation and tunnel effect when large scale integrated circuit is needed [21]. Furthermore, the silicon-based devices are with less transparency due to the narrow bandgap [22], which is not suitable for the circuit. The development of high performance electronic devices is required because of considering the inherent limitations [23]. Flexible electronic devices with a reasonable transparency are expected to meet demands of memory technological in communication, portable display, identification products and computational, where silicon-based electronics cannot provide a solution [24].

The high-performance device is employed for the sufficient use as a transistor in solar cells [25], current-driven electronic circuits [26-28], sensors [29-31], displays [32,33], bioelectronic devices [34] and memory devices [28,29]. At this stage, two main form of the transparent electronic devices, organic semiconductors [35-37] and hydrogenated amorphous silicon [35,36,38] have been widely studied. Researchers have fabricated thin-film transistors (TFTs) and flexible solar cells[23,24,35-38] based on these two formats. Table 1 below lists the field effect mobility (μ_{FE}) of some typical channel materials. [24,39]

Table 1. Field effect mobility (μ_{FE}) of channel materials [39]

Channel Materials	μ_{FE} ($\text{cm}^2\text{V}^{-1}\text{s}^{-1}$)
Hydrogenated amorphous silicon	~1
Pentacene thin film	1.5
Pentacene single crystal	~2.7
Polycrystalline silicon	~100
Single crystalline silicon	~200

It can be seen that carrier mobility of single crystalline silicon is larger than the hydrogenated amorphous silicon. And the difference between this two is nearly 2 or 3 orders of magnitude. The band conduction and jumping in between the localized band tail state result in the carrier transportation in hydrogenated amorphous silicon, thus lead to the large difference. A strongly directive sp^3 orbitals in the covalent semiconductors cause a structural randomness. The bond overlap degrades rapidly with a bond angle fluctuation, thus the carrier transports in a strict direction. High density tail-states can be reached by altering the electronic levels along with bond angle fluctuation. Moreover, a high mobility, define as $\mu_{FE} > 10 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, can be reached in typical amorphous oxide semiconductors that contains post transition metal cations, with an influence of retrogress of band conduction. [40]

2.2 Memristor in Wearable Devices

2.2.1 Introduction of Memristor

An efficient method in terms of speed and volume of computation is to build the network on purpose-built complementary metal oxide semiconductor (CMOS) integrated circuits [41,42]. A field effect transistor (FET) is involved in the circuit. It uses a gate, the input terminal where voltage is applied, to control the current flowing through it. The operation relies on the electric field which is generated by voltage of the gate [43]. When gate input is electrically insulated from the main current carrying channel, the transistor becomes an insulated gate field transistor (IGFET). The most common type of IGFET is the metal oxide semiconductor field effect transistor (MOSFET) [44]. (Figure 1)

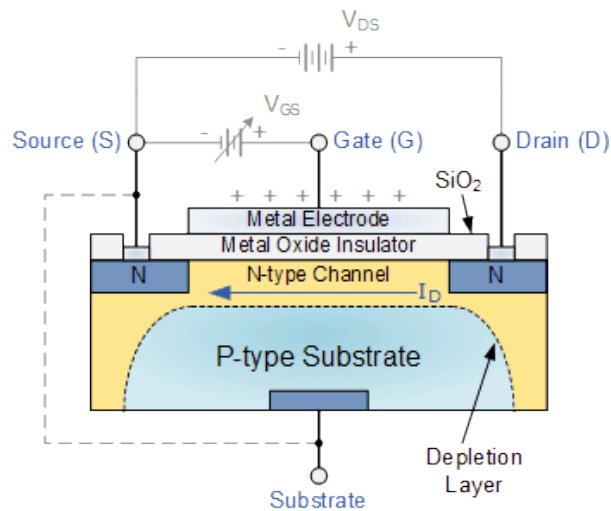


Figure 1. Basic Metal Oxide Semiconductor Field Effect Transistor[44]

It is a combination of two types of metal oxide semiconductor (MOS): n-channel MOS (NMOS) and p-channel MOS (PMOS) [45]. This leads to CMOS only draw negligible leakage currents in standby operation.

To improve the performance of CMOS circuits, a memristor, work as a two-terminal electrical component keeping the correlation between the magnetic flux and electric charge, has been found [46]. This concept was first come up with Leon Chua in 1971 [47]. The idea was that the memristor is worked as the fourth fundamental electrical circuit elements, in addition to resistors, capacitors, and inductors [47]. The I-V graph (Figure 2(b)) called a ‘pinched-hysteresis loop’ is the footprint of a memristor. [48,49]

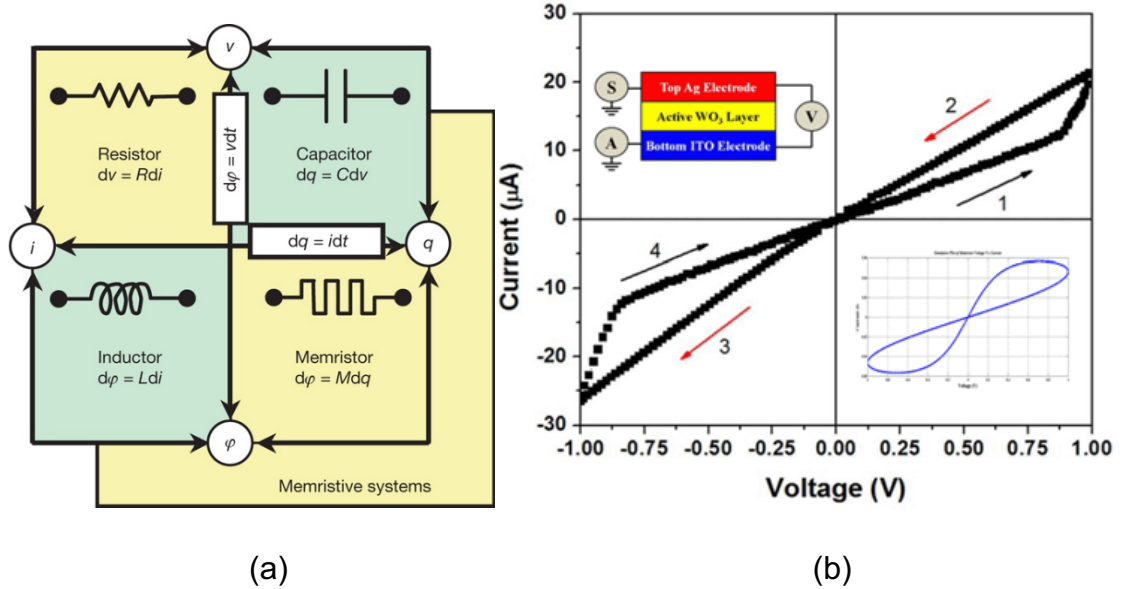


Figure 2. (a) Four fundamental circuit elements (b) Pinched-Hysteresis Loop [46,50]

Memristor is the combination of ‘memory and resistor’. It is a memory circuit element with the function of remembering its previous resistance history [51]. The memristor can change the resistance based on the voltage change during switching on and record the resistance states after turning off the power [52]. In addition, one single memristor take the same task instead of multiple transistors and expresses in the same route of logical computation as it recorded.

The first working memristor is made by Hewlett-Packard (HP) labs in California, in 2008. This memristor has a sandwich structure of Pt/TiO₂/Pt and with a size of 15nm half-pitch whereas the transistor is still of a size of 20nm in width [53]. Nevertheless, memristor requires less energy consumption and is much faster than the flash storage.

The capacity of the CMOS circuits can be improved by using both transistors and memristors. It has been widely accepted that memristor could be a possible alternative element for most current storage devices [15].

2.2.2 Resistive Switching Behaviour

The memristance is a property of an electronic component [54]. It can be shown as a resistive switching phenomenon, which the dielectric varies its (two-terminal) resistance due to subjecting to an external electric field or current [55]. The switching phenomenon usually comes with a non-volatile and reversible characteristic [56,57]. Resistive switching phenomenon was found by Hickmott in 1962 [58] who reported the current-voltage relationship of a metal-insulator-metal (MIM) structure. Several combinations of samples were used in his experiment such as Al/SiO/Au, Al/Al₂O₃/Au, Zr/ZrO₂/Au, Ta/Ta₂O₅/Au, and Ti/TiO₂/Au. [58,59]

The resistive switching between the low resistance state (ON-state or LRS) and high resistance state (OFF-state or HRS) is electrically reversible [60]. The switching from HRS to a LRS is called a 'SET' process, while the reverse is referred as a 'RESET' process [60]. Figure 8 represents two typical switching phenomenon: bipolar switching and unipolar switching, which are classified based on the property of electrical polarity during SET and RESET operation. [60,61]

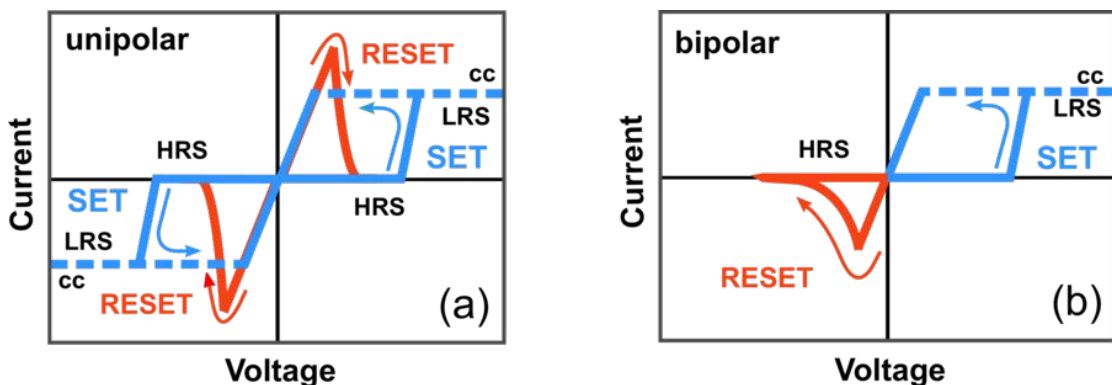


Figure 3. Schematic for basic resistive switching operation (a) Unipolar switching. (b) Bipolar switching [62]

Unipolar switching exhibits high resistance stage and low resistance stage under the same polarity. This means that the switching direction is due to the magnitude of the external input voltage [63]. The voltage at SET state is always higher than the voltage of RESET, and the RESET current is lower than the current compliance (CC) all the way along the SET process [64]. CC is required when conducting the SET operation which is in order to stop the device from a permanent breakdown. For bipolar switching, one polarity of the voltage is needed to switch between OFF-state and ON-state; the opposite polarity is required to switch backwards [65]. The current change for two switching operation can be seen in Figure 9. Thus it can be seen that switching from unipolar mode to a bipolar mode for a semiconducting oxide rarely happened. [63]

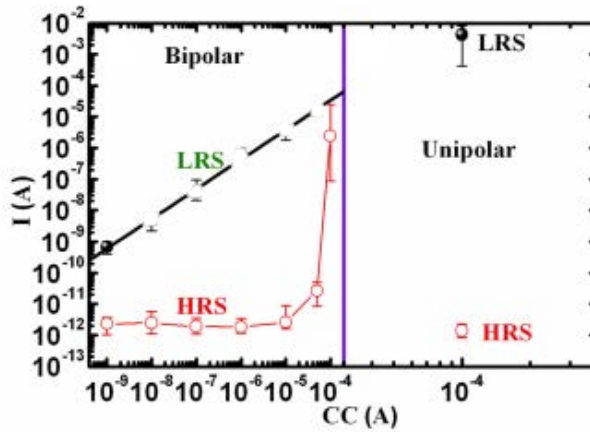


Figure 4. Currents (LRS and HRS) versus CCs under (a) bipolar (b) unipolar mode [64]

For a typical resistive switching device, it requires an electroforming process regardless of the materials used. The forming process, during which metal ions are injected and cause structural modifications inside, creates localized

conducting filaments and results a discrete, abrupt conductance jumps [66] (Figure 4). The semi-logarithmic scale is taken for the ‘pinched-hysteresis loop’ [47] thus results a butterfly shape (indicate on bottom right of Figure 4). The arrows indicate the sweep direction.

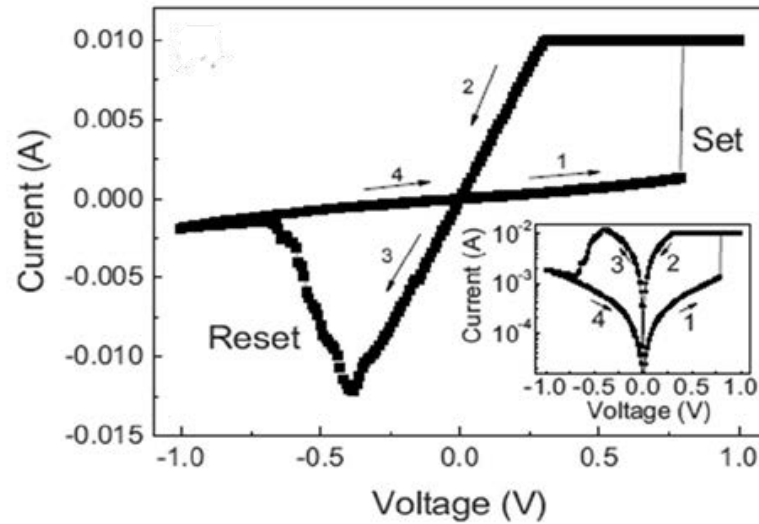


Figure 5. *I-V characteristics of a typical RRAM structure device [61]*

2.3 Mechanisms of Memristor

The memristor attracted scientist's attention since 2008, that Hewlett-Packard (HP) labs in California built the first working memristor with Pt/TiO₂/Pt structure. [53] The key research for the memristor includes its characteristics, physical properties (especially electrical properties) as well as its materials properties. Although researchers keep on studying the fundamental science underlies the switching mechanism of memristor, this topic of research remains challenging. Scientist create several different models to explain the resistance switching behaviours described above. Among these theoretic models, three models are the most widely accepted by the researchers: Schottky Barrier Model, conducting filament model, oxygen vacancy model. [40,60,67]

2.3.1 Schottky Barrier Model

In this model, the resistance change is due to the change in Schottky barriers. The resistance changes occur at top (non-ohmic) interface of the memristor and change between HRS and LRS can be controlled by the height on the Schottky barrier at the interface of the memristor [40]. For a Pt/Ti/TiO₂ structure, the Schottky barrier exists on the Pt electrode and the TiO₂ thin film and the ohmic contact occurs between Ti and TiO₂ interface. When apply an electric field, the device is in low resistance state, the Schottky barrier is very weak and sometimes disappeared. Similarly, for a high resistance state, the Schottky barrier appears more outstanding than the low resistance state. According to this phenomenon, the oxygen ions migrated towards anode along the applied

electric field and the concentration of the oxygen vacancies increase rapidly at the negative electrode interface. Thus, the Schottky barrier starts to disappear and the low resistance states occur. Reversely, a positive voltage applied and lead the oxygen vacancies move back towards the Pt electrode and recover the Schottky barrier, thus a high resistance state can appears.

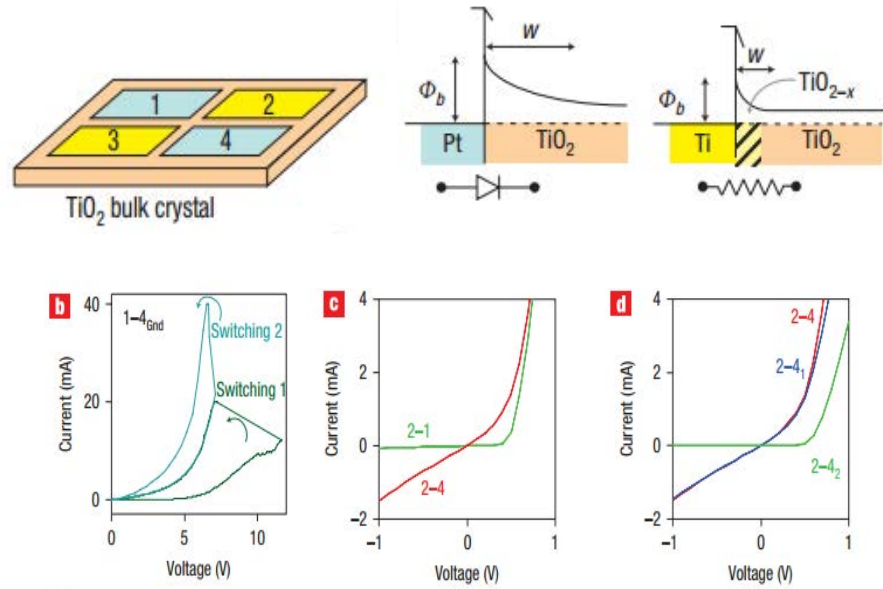


Figure 6. (up) Schematic of the electrode and Schottky barrier (below) Switching occurs at the Pt/ TiO_2 interface [40]

2.3.2 Conducting Filament Model

The conducting filament model is the first model that describe the resistance switching effect and the most widely accepted one. The conducting filament model suggests that when a threshold voltage is applied, the filaments can be created by the voltage breakdown in the dielectric material. The SET process (ON state) occurs when the conductive metallic filamentary conducting path is created. As a result, the resistance of the device changes from high resistance state (HRS) to low resistance state (LRS) [61]. With the time of the voltage

applied, a thermal effect occurs, namely, Joule heating, the filaments are ruptured and the RESET process (OFF state) take place, the resistance becomes a HRS. The overall process results a unipolar behaviour. [55]

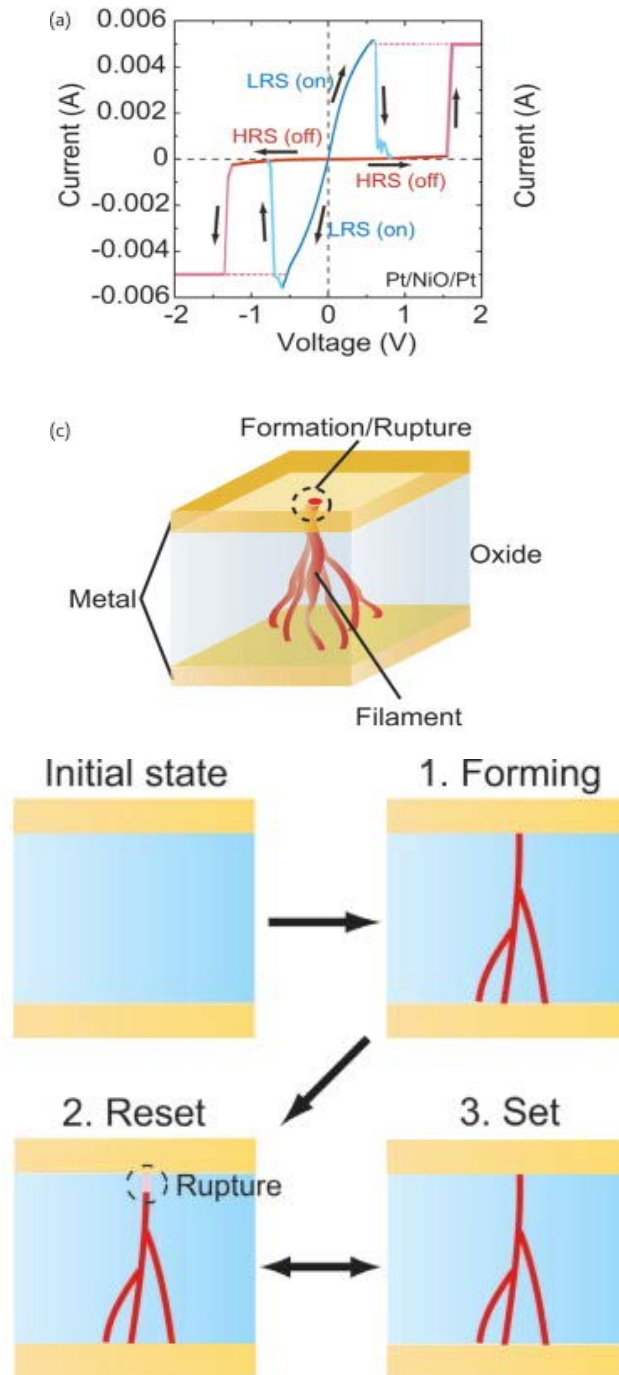


Figure 7. (above) (a) unipolar (nonpolar) switching in a Pt/NiO/Pt cell and (c) a filamentary conducting path (bottom) Schematics of the initial state (as-prepared sample) and (1) forming, (2) reset, and (3) set processes. [55]

2.3.3 Oxygen Vacancy Model

For a transition metal oxide (TMO) based memristor devices, the oxygen vacancy model is the most common explanation for the switching mechanism. A conductive filament formed when oxygen ions (or oxygen vacancies) migration occurs on both electrodes. The migration of oxygen vacancies (each oxygen vacancy has two positive charges) near the defect location along the grain boundary, resulting a large amount of oxygen vacancy defects. The anions migration is the migration of oxygen vacancies. The oxygen vacancies form hopping conduction path, like the filament model, the dielectric material breakdown then the migration of the vacancies creates the filament and SET process (ON state) takes place. For the RESET process to take place, the depletion of electrons in oxygen vacancies along the filaments to recover vacancies. Another mechanism of the anion migration is that the oxygen vacancies acts as the dopants and make the metal oxide layer conductive. The oxygen vacancies then pill up near the cathode and trapping electrons, thus the metal valency reduced and generated the filaments to move up to the anode [68,69]. Similarly, the cations migration is the migration of metal cation. In conclusion, the conductive filament in TMO based memristor devices can be formed through interconnection of the oxygen vacancy defects and caused the migration of the oxygen ions which is induced by the action of the strong electric field (voltage applied). [70] The negative voltage can be applied, and the filament is fused, which work as a restoration process of oxygen vacancies.

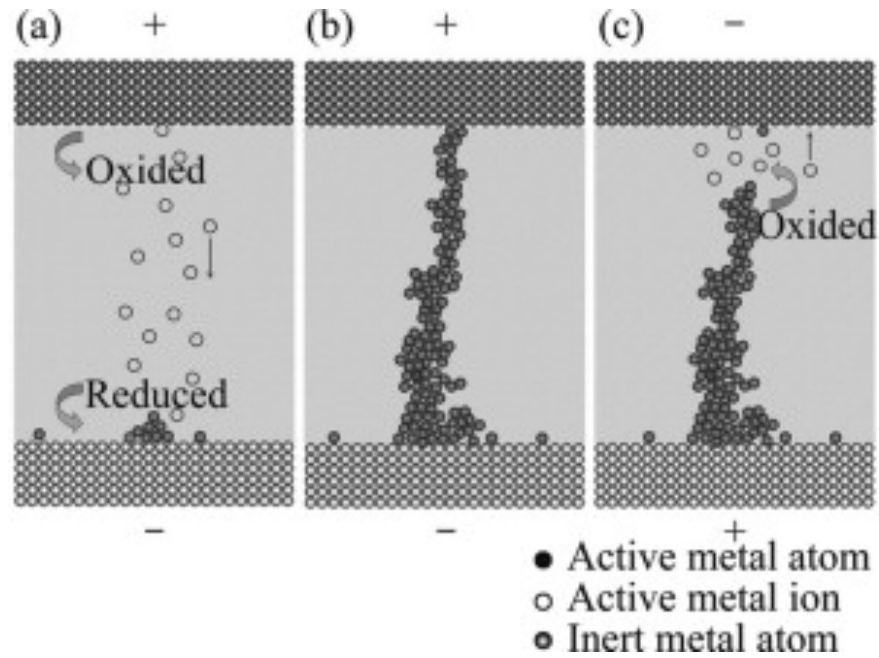


Figure 8. A schematic diagram for mechanism of resistive switching effects in electrochemical metallization cell: (a) metal atoms oxidized at the anode and migrated to the cathode and deoxidize therein; (b) form conductive filament in the cell (c) when voltage is reversed, the breakdown of the filament takes place, HRS occurs. [71]

2.4 CeO₂ Based Thin Film

2.4.1 Properties of Cerium (IV) Oxide

Cerium(IV) oxides (CeO₂ or ceria) is a binary solid oxide of the cerium, a rare earth metal, with a powder form of a pale yellow-white colour [72]. CeO₂ has been recently investigated for multiple applications, such as automotive exhaust catalyst, strong oxidant, insulating layers for silicon-based electronic device, oxygen conductor of the solid oxide fuel cells and working as a high refractive index material layer [22,73-76]. CeO₂ has a fluorite structure, at room temperature, the lattice constant is 5.411 Å. The stoichiometry ratio of the cerium oxide can be reduced from Ce⁴⁺ to Ce³⁺ (i.e. CeO₂ to Ce₂O₃), since the reactivity of the oxide depends on its oxidation states. The schematic figure of CeO₂ unit cells shows that with a stable oxidation states each Ce⁴⁺ cation is surrounded by 8 equivalent distance of O²⁻ anions forming at the corners of a cube. In addition, for each O²⁻ anion, it is surrounded by a tetrahedron of four cerium ions.

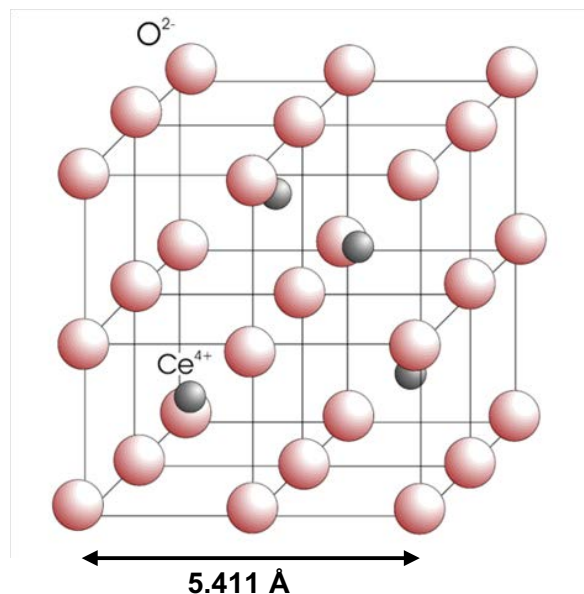


Figure 9. Schematic of CeO₂ unit cell [77]

CeO₂ is very stable even at a very high temperature (melting point: 2600 °C [78]) because of the fluorite structured oxide material with a strongly ionic bonding. The formation of lattice oxygen vacancies in CeO₂ leads an important role in the oxidation of CO and is associated with the reduction of Ce⁴⁺ ions to Ce³⁺ ions. From the viewpoint of increasing electrical activities, it is important to synthesize CeO₂ nanocrystals with ordered structural and highly stable facets, namely, {111} facets based on theoretical calculations that is the most stable surface among the low index planes [79], which would offer the utility in accommodating oxygen deficiency and result in the semiconducting properties with a n-type characteristic ($E_G \approx 3.5$ eV) [80].

2.4.2 Self-assembly of CeO₂

Various preparation methods of CeO₂ nanocrystals have been reported. These methods involve different preparation temperature and environmental requirements, such as precipitation, combustion, thermal decomposition, spray pyrolysis, urea decomposition, electrochemical synthesis and microemulsion [81-86]. High temperature fabrication methods are frequently used for the previous synthesis strategies of CeO₂. As there exists a trade-off between the temperature and the particle size, an ultrafine CeO₂ powder can be prepared and help decreasing the sintering temperature from 1500°C to 1200°C [87]. At room temperature, a range of 3-12 nm size of CeO₂ nanoparticles have been formed by mixing directly with the same volumes of Ce(NO₃)₃ and hexamethylenetetramine [88]. Recently, hydrothermal process was developed

as a synthesis method for preparing CeO₂ nanoparticles [89]. Oleic acid and other organic solvents were added as stabilizing agents during the reaction of forming nanoparticles to improve the self-assembly of the resulting particles. Other factors such as the concentration of the reactants, the water/toluene ratio and the water/oil surface can influence the reaction as well. Nanocubes is considered as the most stable form of the nanoparticles, which is promoted for the preparation process for the CeO₂ for the thin film fabrication. [90]

2.4.3 Synthesis Methods of CeO₂ Nanocrystals

Both shape-controlled and size-controlled synthesis of ceria nanocubes can be tuned more conveniently by several factors. The amount of surfactant is one of the most remarkable factors to control the reaction system. The dispersion between nanoparticles will be evaporated with time past and yields an assembled pattern. The presence of oriented aggregation mediated precursor growth leads to great structural properties with synthesized CeO₂, which are extremely intriguing for the application of insulating layers for silicon-based electronic device. The hydrothermal and solvothermal process was frequently used to prepare the CeO₂ particle. The reaction conditions for these two methods require a high boiling temperature medium, high temperature and high-pressure environment [91-94]. The aqueous solution of Ce(NH₄)₂(NO₃)₆, an inorganic precursors of metal salts [93], is used for the sol-gel method of preparation for the cerium oxide nanomaterials.

A microemulsion method has been used as a new synthesis strategy of CeO₂. The microemulsion is a reverse micelles process and the system consists of a continuous oil phase like oleic acid, a surfactant and a dispersed phase such as a aqueous solution [93]. Oleic acid is using as a surfactant to form the stable monodispersed CeO₂ nanoparticles in hydrocarbon solvents. The decomposition of cerium-oleate complex is conduct under a high boiling point in different solvents and formation of CeO₂ nanoparticles can be processed. The cerium-oleate complex can be created by reacting cerium chloride heptahydrate with the sodium oleate in a mixture liquid of ethanol, water and hexane at 70°C

for 4 h [95]. An oil-liquid layer can be identified after the reaction was completed, the upper layer, a mixture of organic component, with the cerium-oleate complex then can be dissolved in the high boiling point solvents and used for thin film fabrication. The table below shows the results for dissolving oleic acid and cerium-oleate complex in different high boiling point solvents. The particle size can be controlled by the reflux condition, especially the high boiling point solvents. A longer reaction time and higher solids concentration would obtain a larger particle size.

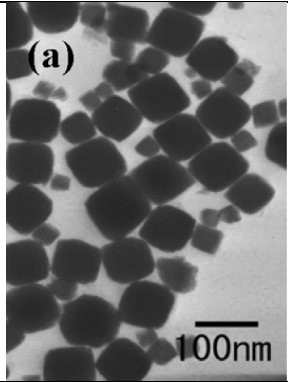
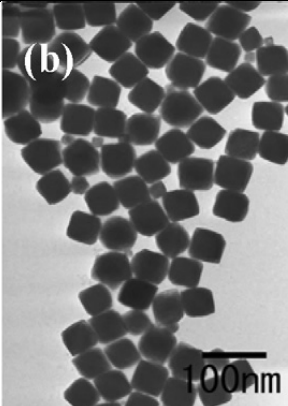
Table 2. Effect of high boiling point solvent on particle size of CeO₂

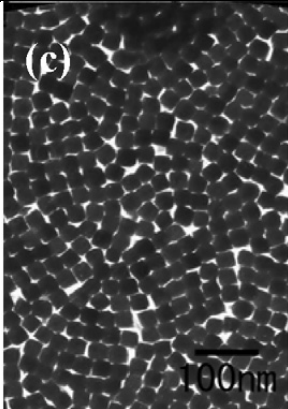
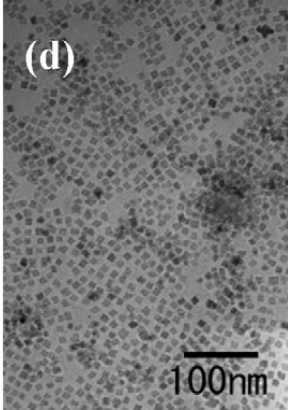
Solvents	Boiling point (°C)	Reflux Condition	Result solution	Particle size (nm)
Octyl Ether	290	Up to 290°C for 4 h	Dark brown, contained 1 wt % solids	10-20
1-Tetradecene	251	Up to 250°C for 2 h	Colourless, contained 1 wt % solids	10-20
Decalin	189-191	Up to 180°C for 1 h	Pale yellow, contained 1 wt % solids	5-8
		Up to 180°C for 5 h	Dark brown, contained 5 wt % solids	~10
Cosolvent Dipropylene Glycol Monomethyl Ether	185	Up to 185°C for 10 h	Dark brown, contained 1 wt % solids	60-90
Cosolvent Dipropylene Glycol n-Butyl Ether	230	Up to 225°C for 1 h	Dark brown, contained 1 wt % solids	~10
Cosolvent 2,2,4-Trimethyl-1,3-	255	Up to 255°C for 1 h	Yellow, contained 1 wt % solids	30-60

pentanedio Monoisobu tyrate			Dark brown, contained 5 wt % Solids	60-90
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On the other hand, the ratio of surfactant (oleic acid) concentration with cerium precursor can have a drastic effect on the size distribution of the final nanoparticles. Y. Tao et al. report the different ratio of oleic acid (OLA), as surfactant, to cerium precursor ($\text{Ce}(\text{NO}_3)_3$) and its effect on particle size of the CeO_2 nanocube [96].

Table 3. Size of CeO_2 nanocubes based on different ratio of $\text{OA}/(\text{Ce}(\text{NO}_3)_3)$

Ratio of OLA to $(\text{Ce}(\text{NO}_3)_3)$		Average edge length (nm)	TEM images
Concentration of OLA	Concentration of $(\text{Ce}(\text{NO}_3)_3)$		
1	1	125.3 ± 4.2	 (a)
3	1	75.6 ± 2.3	 (b)

6	1	52.1 ± 0.8	
8	1	10.4 ± 0.3	

Oleic acid is not the only additive that can help the self-assembly process. Some organic solvents are added during the microemulsion process to improve the size of the particles. The highly sensitive nano-sized particles can be controlled by adding poly(ethylene glycol) into the precursor solution and thus the grain growth or particle agglomeration can be reduced [97]. A sono-chemical synthesis of CeO_2 nanoparticles using $\text{Ce}(\text{NO}_3)_3$ and azodicarbonamide as starting materials with ethylene-diamine or tetraalkyl-ammonium hydroxide as additives, or in the presence of NaOAc and ethylene glycol (EG) has been conducted. For a room temperature, a semi-batch reactor method was developed for synthesizing CeO_2 nanoparticles [95].

2.4.4 Cracking-free Thin Film

CeO₂ is a transition metal oxide and the preparation of CeO₂ thin film can start with a high-quality control nanoparticle. Furthermore, using different method of fabrication may change the microstructure and the properties of the CeO₂. Different characterization of the thin film is shown with different size and crystalline forms as well. This is due to the different process condition, such as temperature and preparation time, especially the preparation methods are the main reason. There are mainly two methods to use for the fabrication in this research. The structure of memristor has three layers in a sandwich layout. The top and bottom electrode is separate by an insulator layer. Furthermore, recent studies in the insulator layer show that a majority of binary transition metal oxides (TMO) [98] emerging the resistive switching phenomenon (Table 4 below). Thus, the insulator layer is also referred as a transition metal oxide layer and the namely the corresponding structure as metal-oxide-metal (MOM). [98]

Table 4. Layout and alternative materials for the MOM structured memristor [99]

Layers	Material
Top electrode	Pt, Au, Ni, TiN/Ti, TiN, Ru

Transition metal oxide layer	TiOx, WOx, NiOx, TaOx, HfOx
Bottom electrode	TiN, W, Pt, TaN

For a device with MOM structure, the orientation, grain size, a highly ordered structure, crystalline arrange and defects are indispensable for the high mobility. Thus, the optimizing and controlling of quality of the thin films are important for the devices and a cracking-free thin film is required for a better performance. Several different surface treatment methods have been investigated to improve the morphology and the electrical quality.

2.5 UV Treatment

UV/O₃ treatment is normally used as a dry cleaning method to remove the surface contaminants [100]. The MOM with an Au electrode can be treated by the UV/O₃ and the work function of the electrode would increase [101]. This is due to the decreasing of the charge injection barrier and thus leading to a dramatic improvement for the electrical properties of the device [102]. The thin film layers are sensitive to the morphology, crystallinity, deposition parameters and other surface conditions, which will inevitably affect the UV/O₃ treatment and significantly influence the performance of the devices besides the raise in work function. The UV/O₃ treatment can greatly decrease the water contact angle of the thin film layer and the concentration of organic particles of the surface for the thin film. The sample under an ambient condition can be kept clean for a significant long time. With a large thickness of the thin film, the films on UV/O₃ treated substrate would have larger grain size than the untreated samples[103]. Grain boundary can be used as a charge trap and increase the amount of charges and thus increase the grain size. It can be seen that small grains would have low surface energy with a high water contact angle, whereas the large and dendrite grains would involve a low water contact angle and high surface energy [104]. The morphology and the molecular crystal structure will have great effect on the electric characteristics.

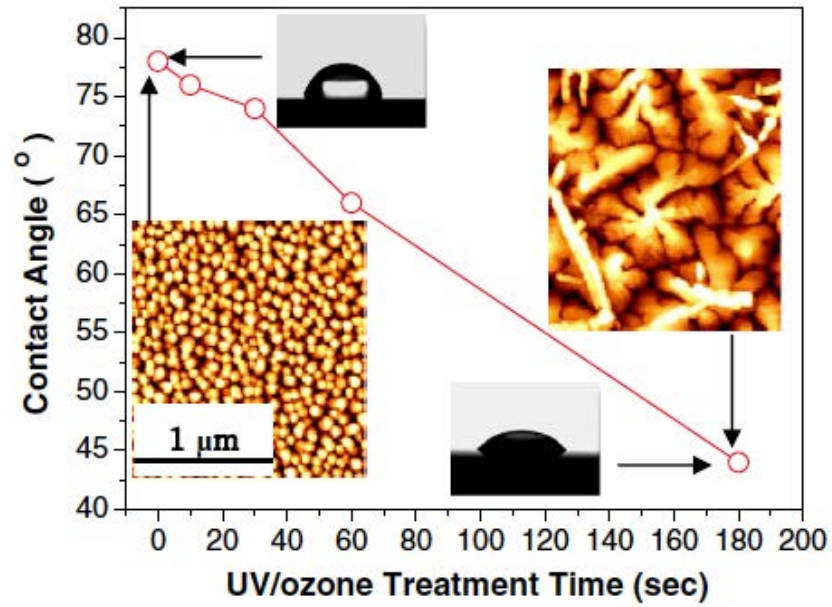


Figure 10. The relationship between UV/O₃ treatment time and contact angle [104]

On the other hand, as afore-mentioned, the organic contaminants can be removed during the UV/O₃ treatment at first and then further exposure caused a dissociation excitation of carbon-hydrogen, carbon-carbon and hydroxyl bonds in near-surface layer of the thin film. The decreasing concentration of the surface contaminant and the hydroxyl groups can be considered acting as electron trap sites. Among the above reasons, the decreasing of surface contamination and increased particle grain size are mainly attribute to the change in device performance with UV/O₃ treatment.

2.6 Plasma Treatment

Cold plasma (or glow discharges) is a surface treatment method for removing the organic contaminant from the surface of the thin film. The plasma can be generated in gases with a low pressure. A sufficiently strong electromagnetic field is applied over the gas under an applied voltage (Both alternating (AC) or static (DC) can be used). Low energy molecular species impinging on the thin film surface and the path from the plasma to the surface does not involve any strong electric fields. The reaction between ions diffused to the sample and the surface particles can form a reaction product for desorb from the surface then finally pumped away from the surface. The surface composition is highly uniform after the oxygen plasma cleaning and the power of the treatment is reduced for a shorter treatment time or a lower plasma energy.

Like the UV treatment, the surface treated by an oxygen plasma would be highly polar (i.e. hydrophilic) that is indicated by the decreasing in the water contact angle. The water contact angle for the sample surface after the oxygen plasma treatment would be less than 10 degrees. Consequently, the residual organics, which is the main source for the contamination, is reduced with the decreasing water contact angles. The polar groups such as carbon-hydrogen, carbon-carbon and hydroxyl bonds can be formed under oxygen gas atmosphere, which is very active, and the surface becomes hydrophilic after the treatment.

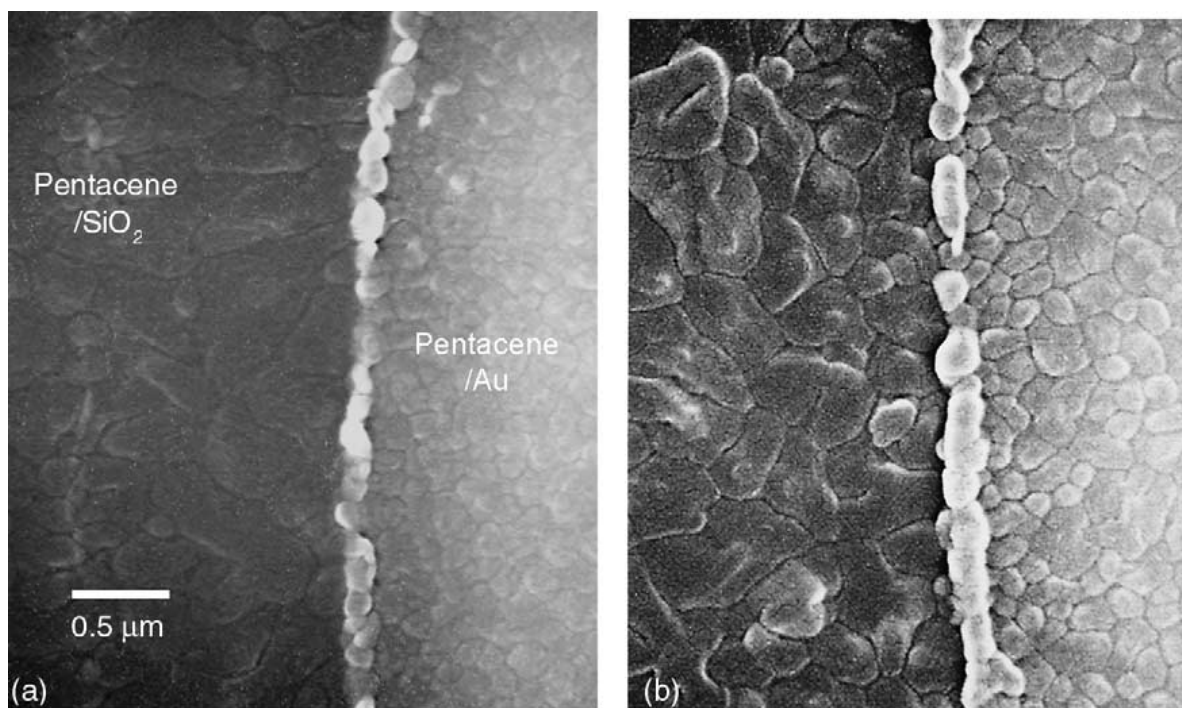


Figure 11. The SEM images of pentacene film deposited on (a) as-prepared, (b) oxygen plasma treated

3. CERIUM OXIDE SUSPENSION INK

3.1 In-doped CeO₂ Ink

Cerium(III) nitrate hexahydrate ($\text{Ce}(\text{NO}_3)_3 \cdot 6\text{H}_2\text{O}$) was chosen as the cerium precursors for the experiment. $\text{Ce}(\text{NO}_3)_3 \cdot 6\text{H}_2\text{O}$ is a translucent colourless crystal, the molecular weight is 326.12 g/mol [105]. The concentration of Indium doping was changed (2.5%, 5%, 7.5%, 10% and 15%) and compared in the next section. To prepare a 5% In-doped CeO₂ ink as sample, 0.10333 g of cerium nitrate and 0.00376 g In₂O₃ (indium precursors) were dissolving in 15ml distilled water in a Teflon tube and shake for 1 min. 14.25 ml toluene, 0.6 ml oleic acid (OLA) and 0.15 ml tert-butylamine were mixed in a beaker. The mixture was then slowly poured into the Teflon tube to ensure the liquid-liquid (oil-water) interface. The Teflon tube was installed in a mould and put into the autoclave with 200°C for 36 hours. The upper solution without oil was extracted and followed by the centrifuge process. 2 ml upper solution with 4 ml ethanol were set for each centrifuge tube. The rotate speed was 1600 for 3 min. Discard the solution and left the powder stick on the tube. For each centrifuge tube, added 3 ml toluene or hexane as solvent. The final product was an In-doped CeO₂ ink. Oleic acid was added as surfactant to improve the self-assembly of the CeO₂ nanocube in the solution.

The CeO₂ suspension ink was checked by transmission electron microscopy (TEM) for self-assembly and crystal shape. A solution with cubic shaped CeO₂ nanoparticles was closely packed. This solution was used to fabricate the device ensuring a cracking free thin film.

3.2 CeO₂ Ink Perfection

A hydrothermal fabrication process of CeO₂ ink was taken under 200°C to confirm the shape control of the nanoparticle with temperature effect. Moreover, the cubic shape of a CeO₂ nanoparticles was a special requirement of the ink preparation. The shape of the particles was near polygon and most were cubic shapes. It can be double confirmed from the literature for shape control of the nanoparticles [106].

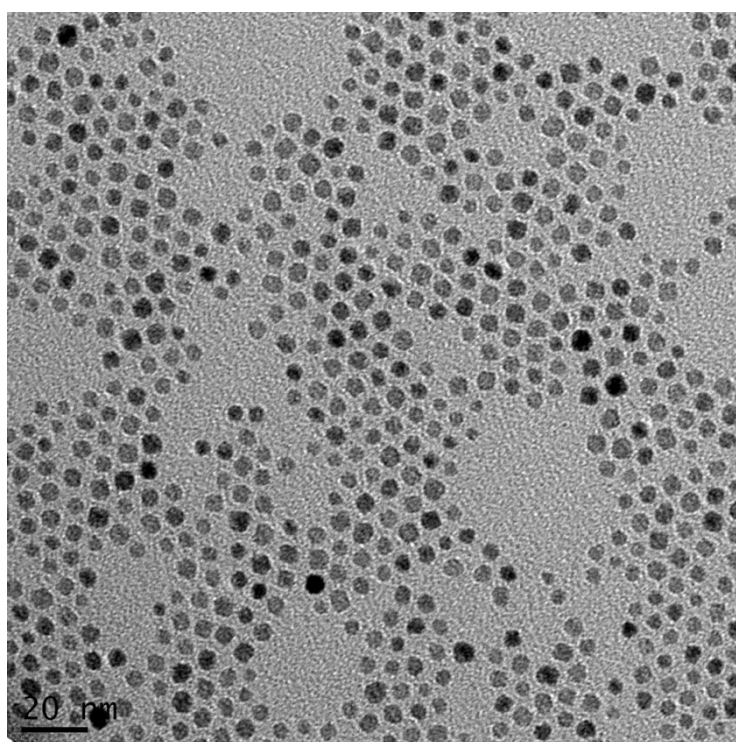


Figure 12. TEM image of In-CeO₂ 200°C

Non-doped and different concentration of In-doped CeO₂ ink were fabricated by the procedure in previous section. The TEM analysis was taken to check the shape of the nanocrystals and ensure the solution with a good self-assembly property. Following figures showed different concentrations of indium doping for the CeO₂ solution.

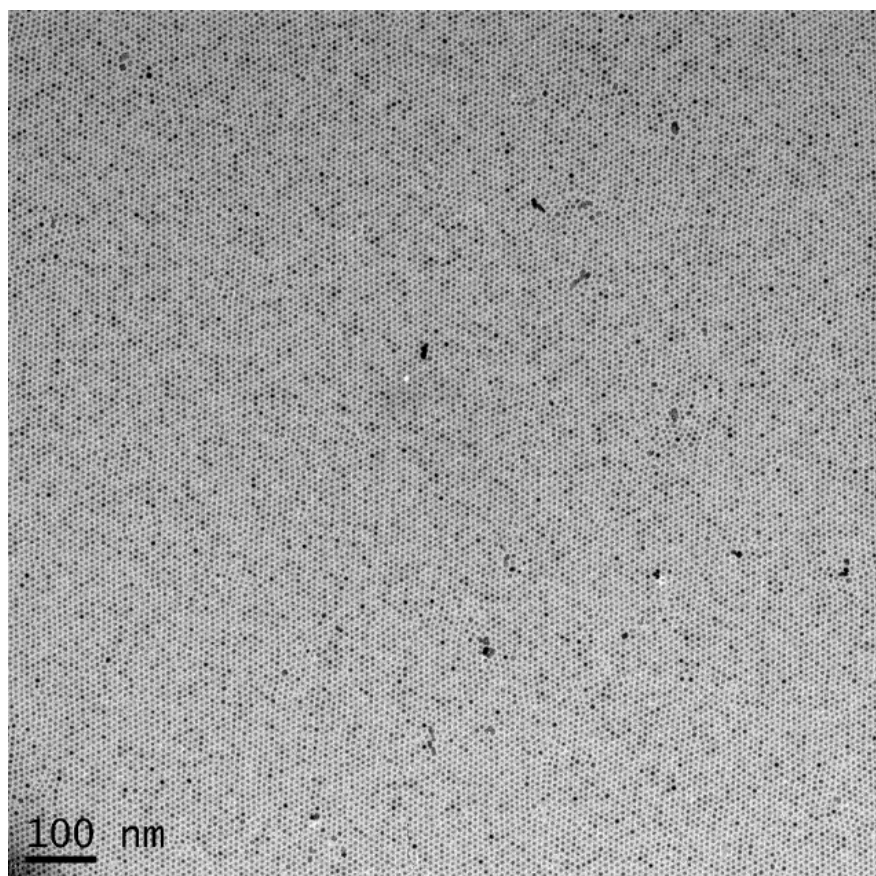
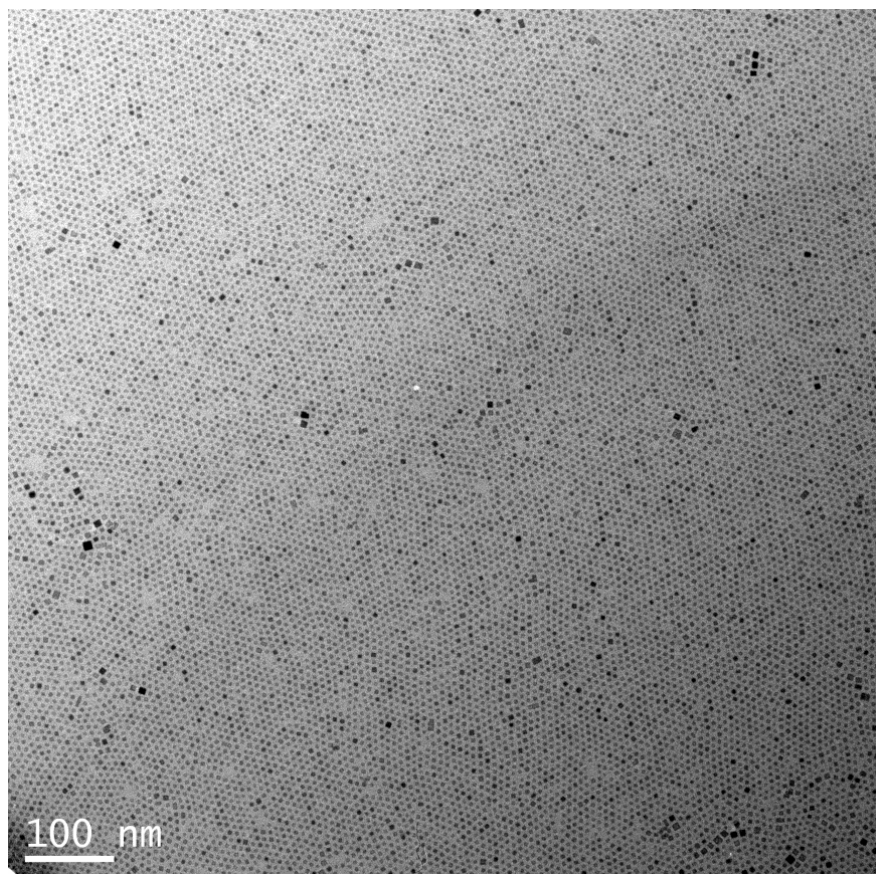


Figure 13. TEM image of (1) 2.5% In-doped ink (2) 5% In-doped ink

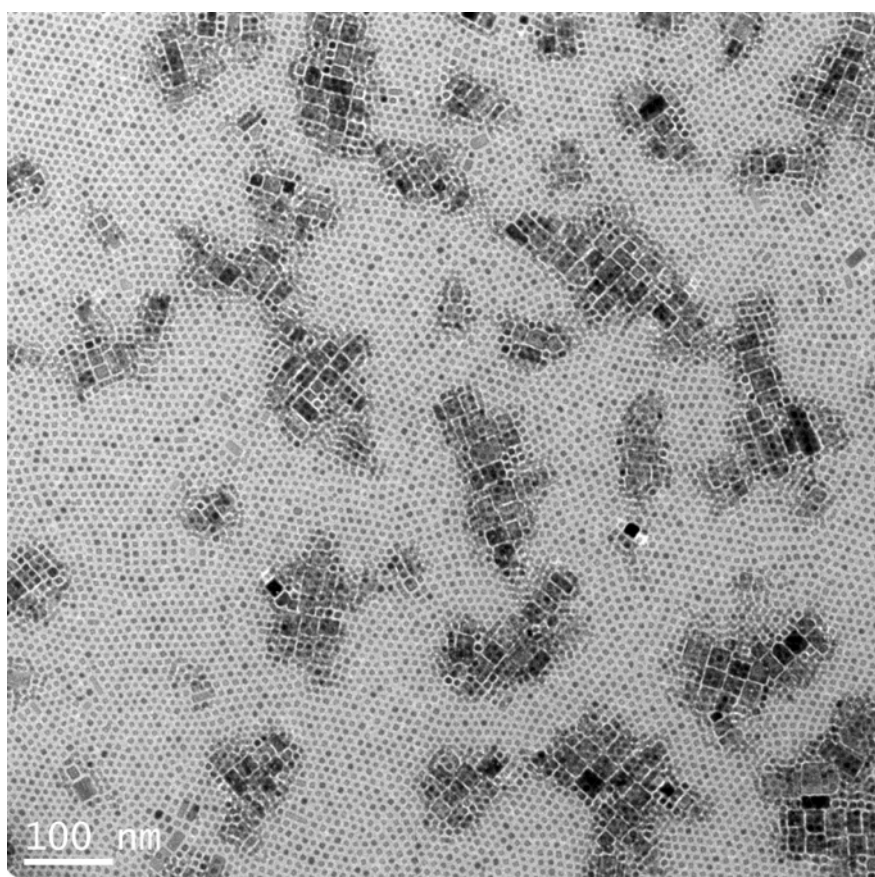
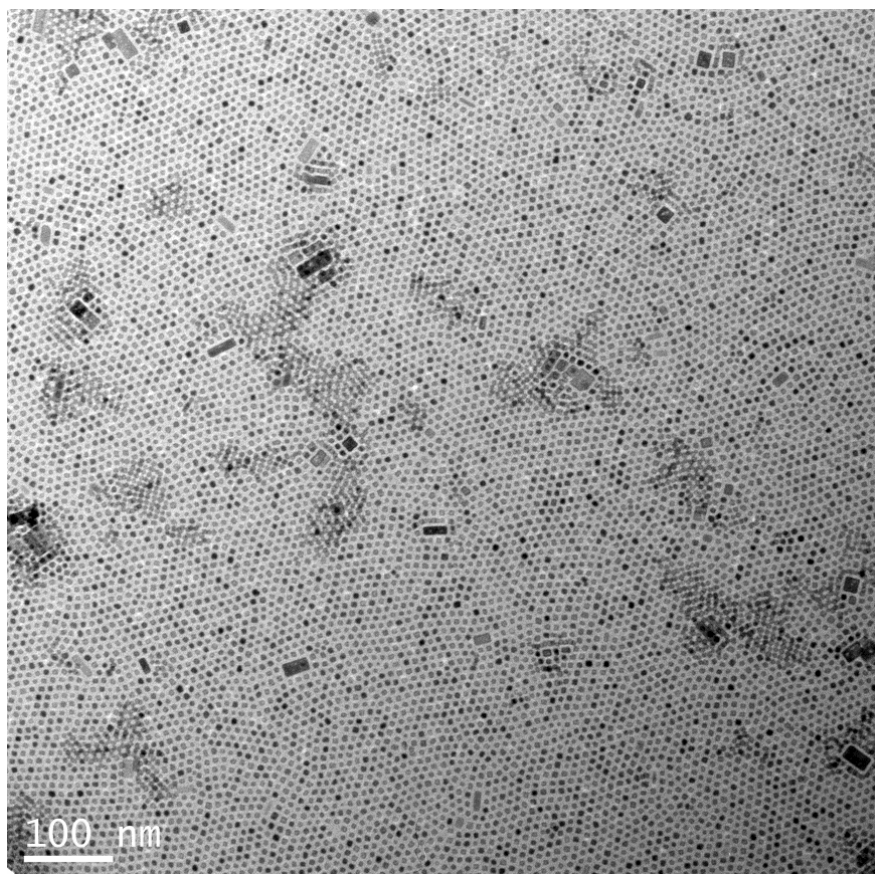


Figure 14. TEM image of (1) 10% In-doped ink (2) 15% In-doped ink

Indium ions are larger than the CeO_2 ions thus shown as larger black dots [107,108]. Indium can be doped into the CeO_2 successfully, but high doping concentration may raise agglomeration of the cube and hence enlarge the local nanoparticles size. Large percentages of doping would reduce the self-assembly due to this cube distortion and thus increase the chance of producing residual power during time [108].

These In-doped inks were fabricated into thin film device for further analyse of effect on the electrical properties. First of all, XRD was used to double confirmed the composition of the thin film (Figure 15). For low concentration of In-doping, nearly no Indium was detected by the XRD whereas high concentration of doping caused a cube agglomeration [109] result in XRD as the $\text{In}(\text{OH})_3$ compound [110].

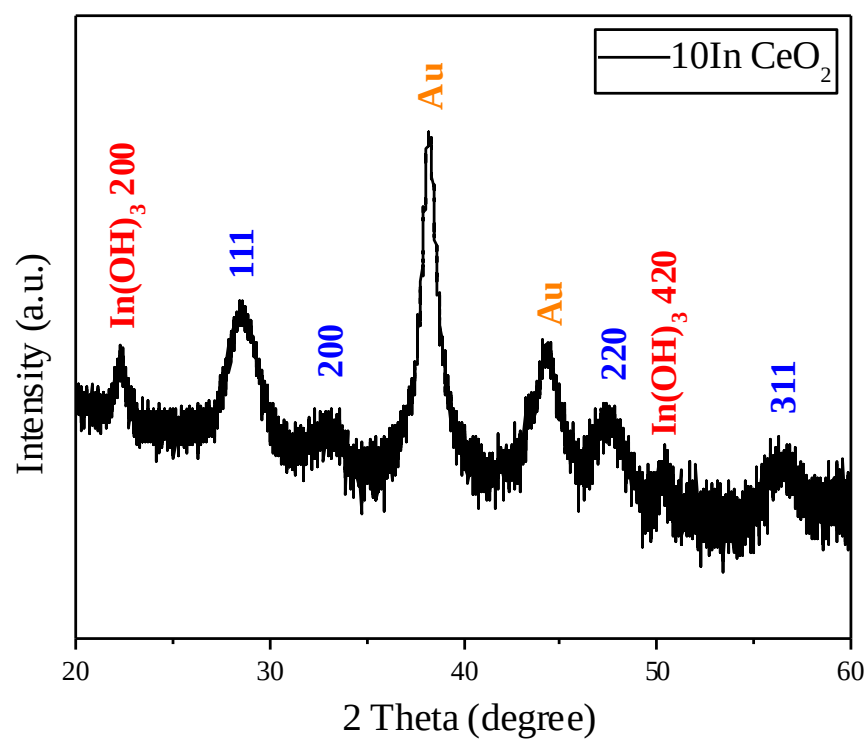
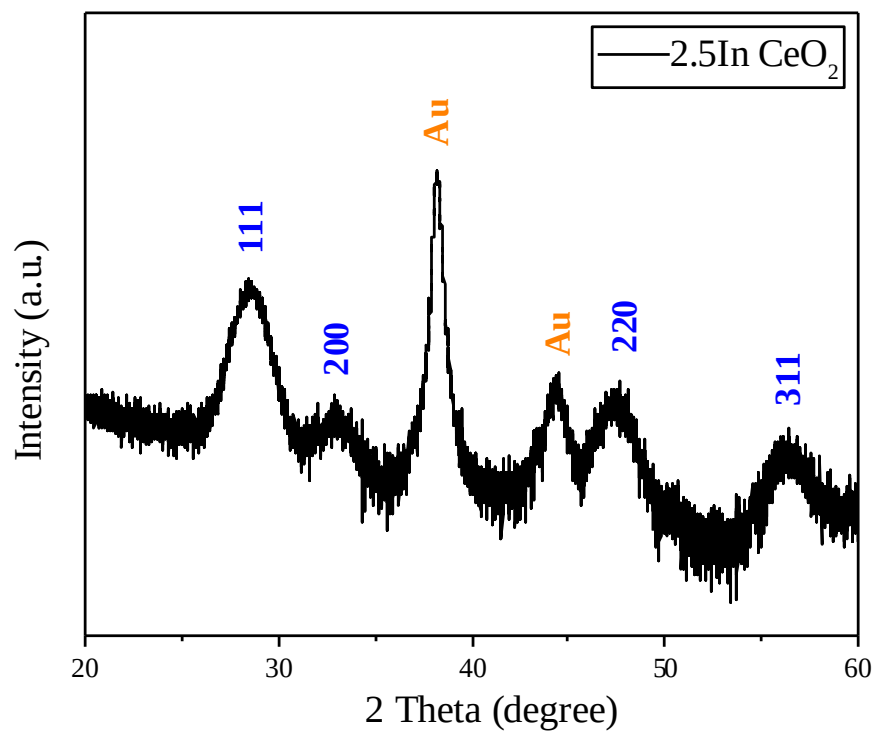


Figure 15. XRD of (1) 2.5% In-doped ink (2) 10% In-doped ink

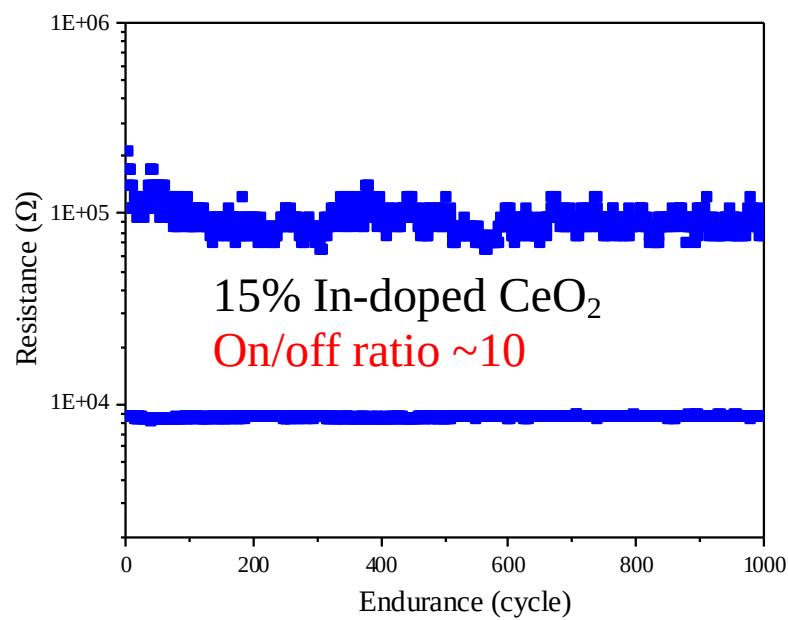
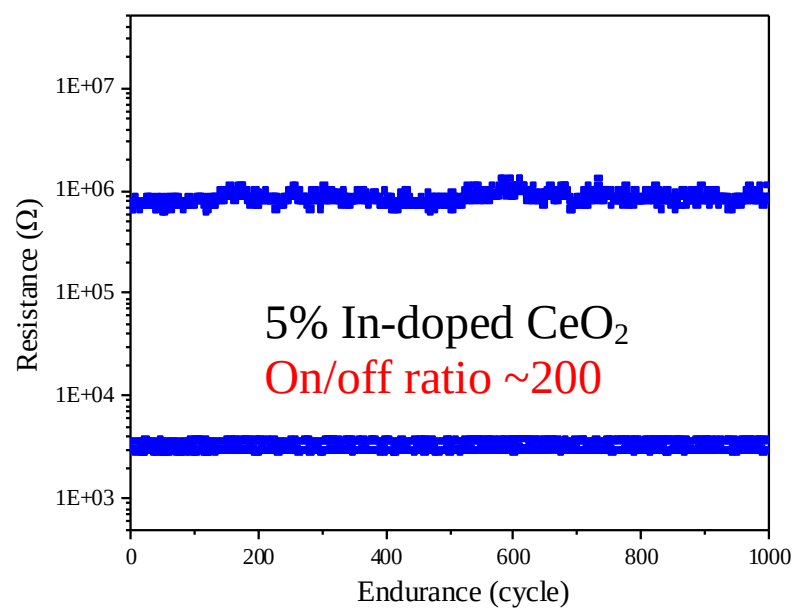


Figure 16. On/off ratio of (1) 5% In-doped CeO_2 (2) 15% In-doped CeO_2 thin film

The on/off ratio for 15% In-doped thin film was around 10. The one with 5% indium concentration had an on/off ratio up to 200. (Figure 16(1), (2)) The on/off ratio decreased as doping concentration increased, because the cube agglomeration increased the obstacles of the electron ions going through thus degraded the electrical performance for the device. The I-V curve for both doping percentage would be used as a proof. It was more stable for the change at 5% than the one with 15%. (Figure 17(1),(2)) The resistance change became unstable during test thus fail to the endurance test.

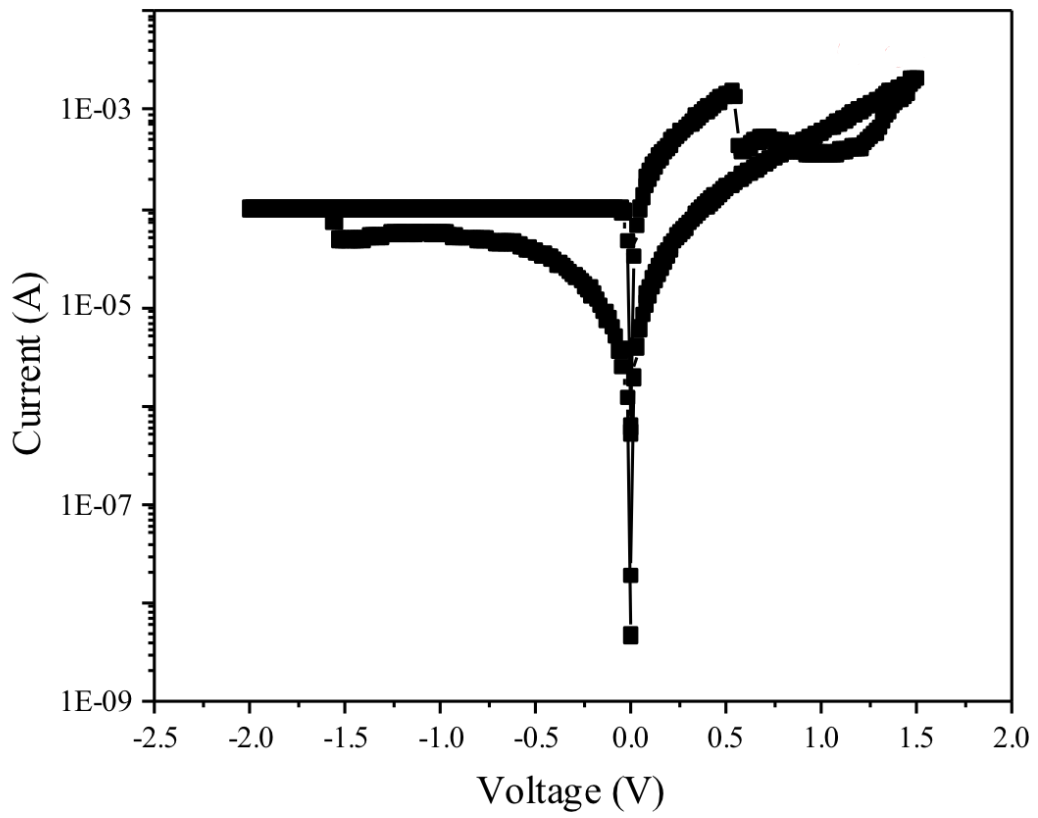
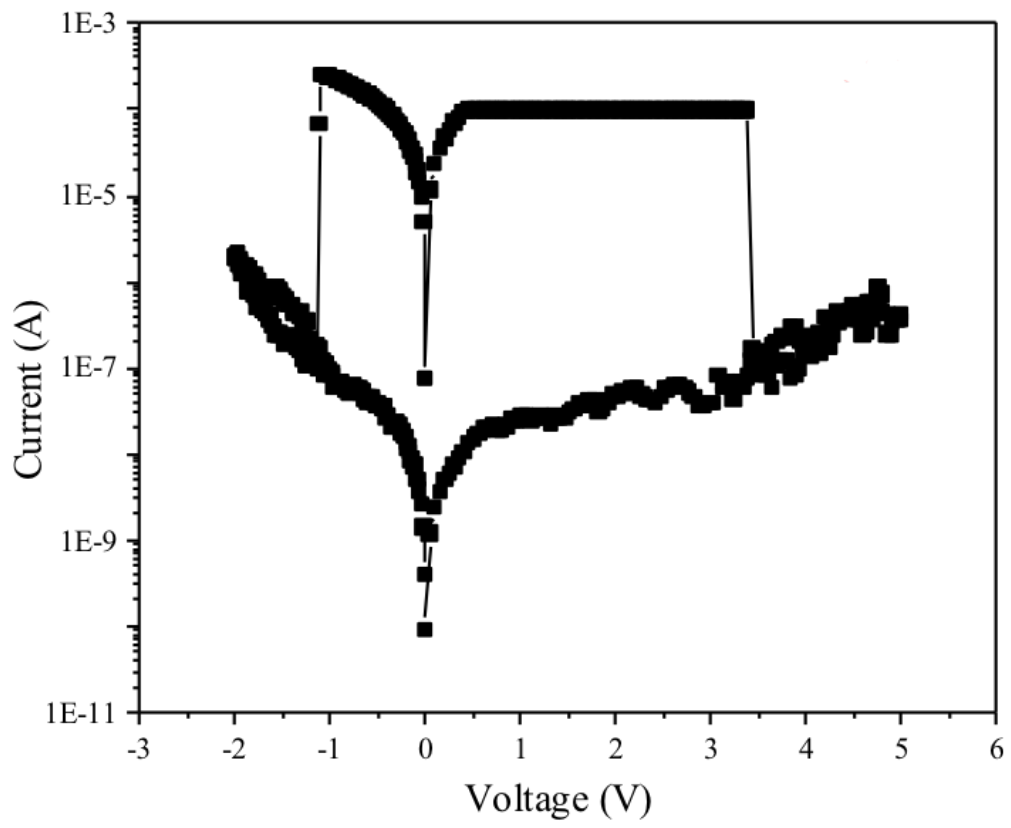


Figure 17. I-V curves of (1) 5% In-doped CeO_2 (2) 15% In-doped CeO_2 thin film

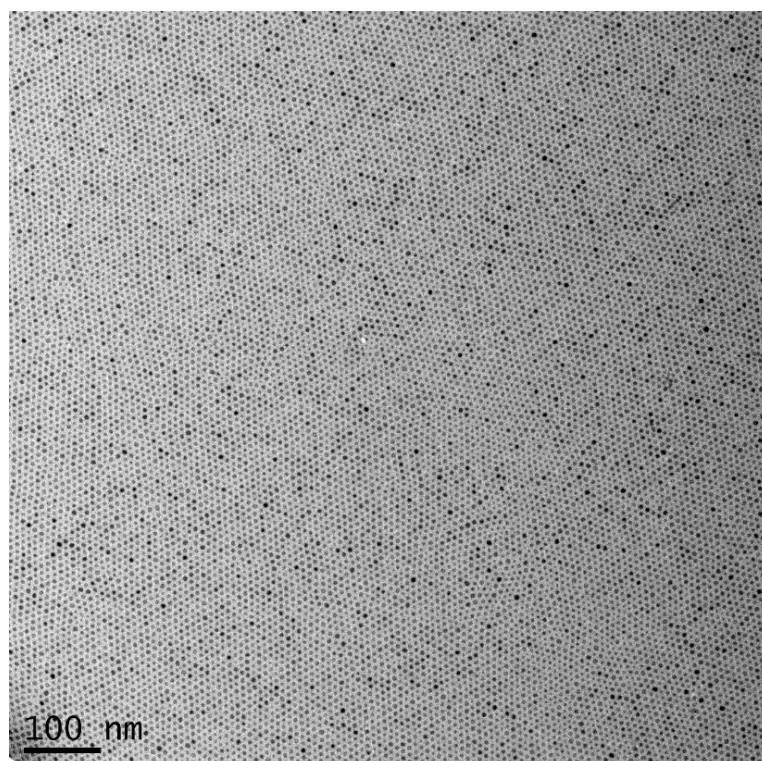
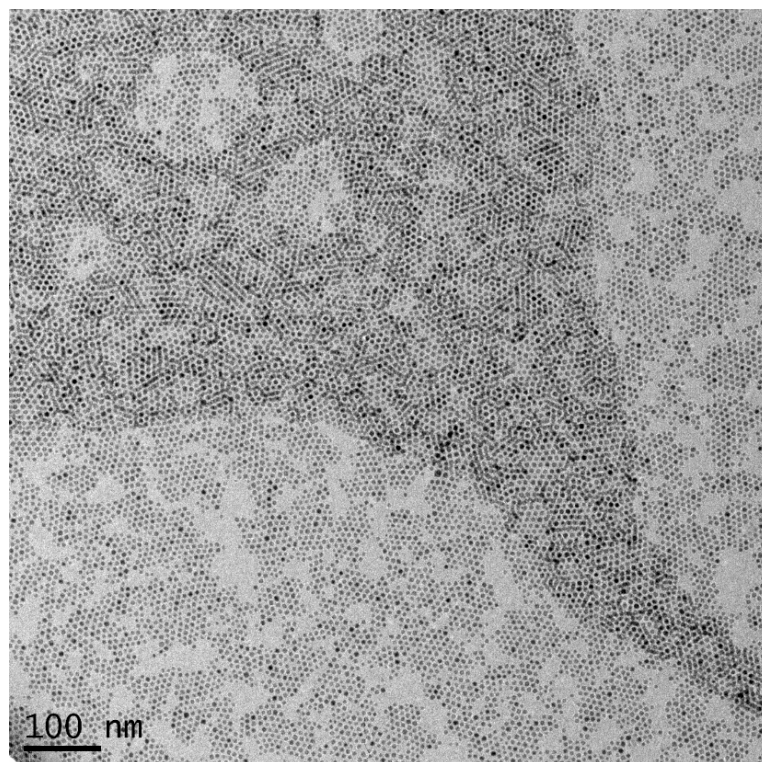


Figure 18. (1) In-CeO₂ without OLA (2) In-CeO₂ with 2% OLA

Similarly, adding OLA after the hydrothermal process can increase self-assembly of the cube. The TEM images show ink with 2% OLA (Figure 18(1)) presents a more closely packed and better self-assembled distribution of nanocubes than that with 1% OLA (Figure 18(2)). Over adding OLA would result a same phenomenon as doping effect. The cube agglomerating occurs when adding excess amount of OLA [111]. An agglomeration can be seen in Figure 19 (1) with the over adding amount of OLA at 2%. The intension of cubic concentration in dark area was stronger than that of in normal areas.

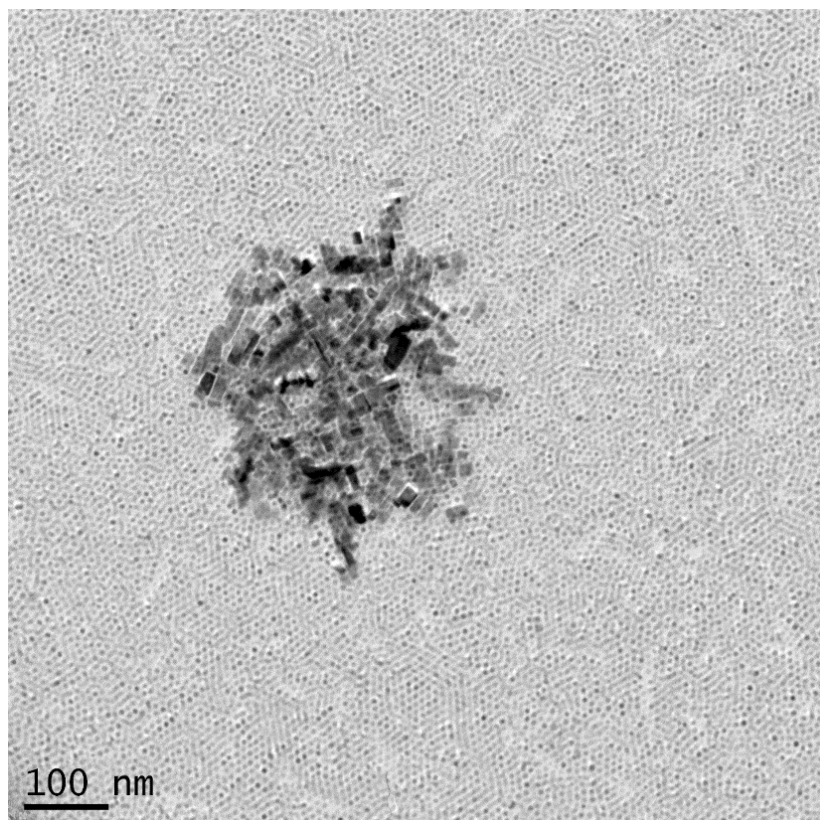


Figure 19. The agglomeration of CeO₂ nanocubes in 1.5 ml toluene with 2% OLA

As the agglomeration occurred in 1.5ml toluene with 2% OLA solution, the other areas of the same sample were poorly compact and with high void content

(Figure 20(1)). The 1.5ml toluene with 1% OLA had more close-packed nanocubes and lower chance of cavity to occurs (Figure 20(2)).

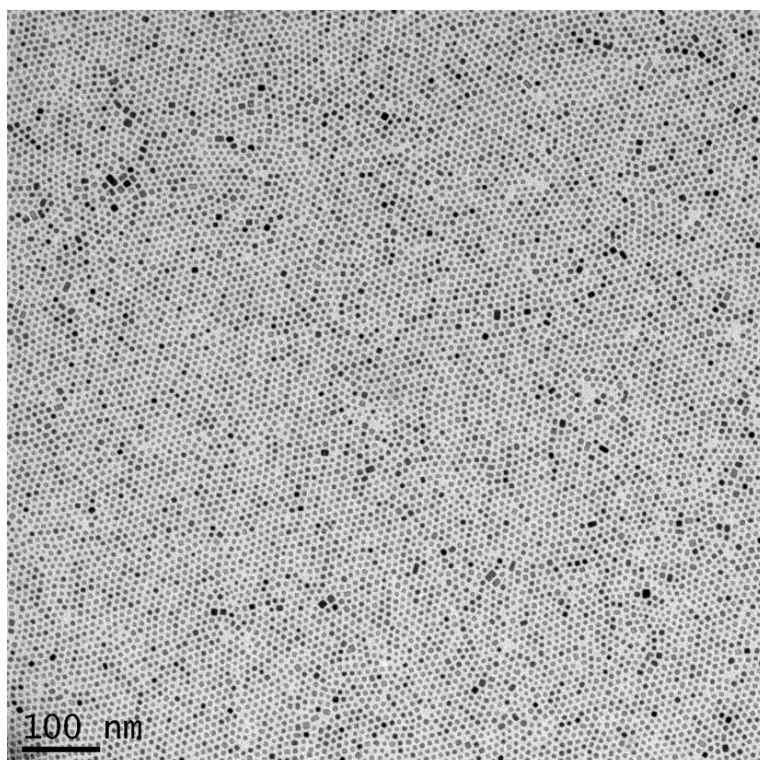
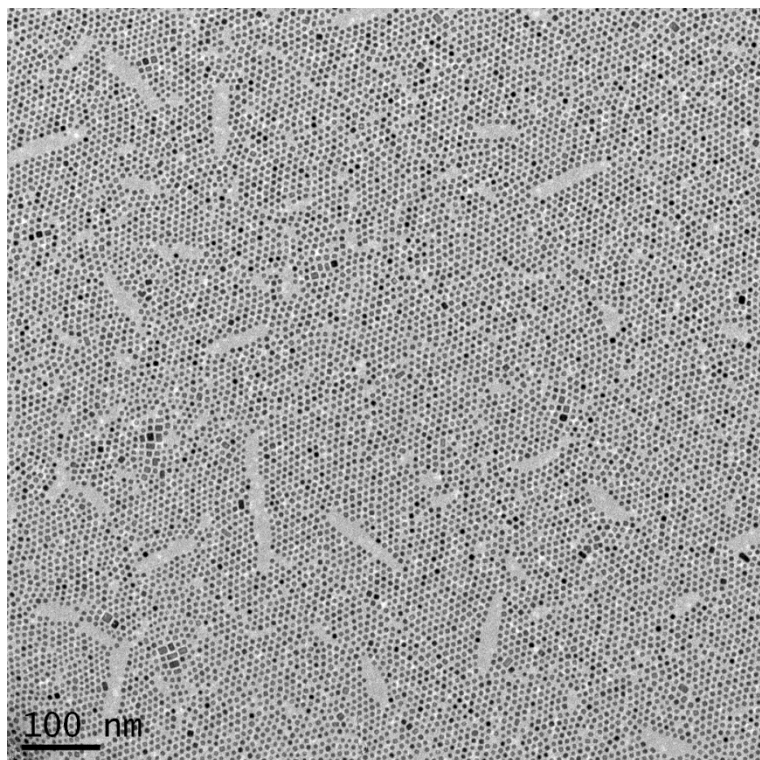


Figure 20. The CeO₂ nanocubes were dissolved in (1) 1.5 ml toluene with 2% OLA (2) 1.5 ml toluene with 1% OLA

4. CERIUM OXIDE THIN FILM DEVICE

Gold/Platinum coated silicon substrate was chosen as the bottom electrode for thin film fabrication. The silicon substrate was cut into a rectangle of 2.5 cm x 1.5 cm in size for each sample. The substrate was washed and cleaned with an ultrasonic cleaner. The cleaned silicon chips were then dried by employing nitrogen gas gun and put in an ultraviolet radiation sterilizer for about 15 minutes to guarantee a clean surface. These substrates were put in a gold sputter at 40 mA for 210 seconds.

The ink was shaken by ultrasonic to ensure the particles were suspended uniformly in the solution. For drop-coating method, one layer contained 10/20 drops ink of 20 μ L per drop. With a spin coating process, the spin coater was set up for one routine at a spin speed of 1000 cycles per second for 20 seconds. A micropipette with a drop of 20 μ L was used for one routine. For one single layer of the thin film, 6 routines were applied. After spin coating for each layer, the plasma treatment was introduced. For a plasma treatment, O₂ were employed, and the power was set at low (7W) for one hour. The layer of thin film was dried during this stage. No annealing process was required as the ink was a crystalized product. Final sample involved in this experiment were of four and eight layers to ensure the thickness and properties for the testing.

A scanning electron microscope (SEM) test was applied to the gold coated substrate to ensure a flat surface and hence reduce the effect to the thin film. An X-ray diffraction (XRD) test was conducted to analysis the composition of

the thin film. The SEM test also was applied for the thin film to analysis the microstructure and morphology. The Focused ion beam (FIB) was involved as a conformation for composition and thickness checking. The sample was covered by a gold top electrode using a special mask before property tests, each electrode of 250 μm in size using a gold sputter as well.

The sample was connected to the Auto-lab by a probe-station; the I-V characteristic was tested through the program. The voltage and current changes were captured for further analysis. The stretching test was conducted during this stage as well. In addition, a digital source meter was employed to test the endurance and retention in a similar way to the Auto-lab program.

4.1 Cracking free CeO₂ Thin Film

4.1.1 Effect of Solvent

A CeO₂ ink with 5% In-doping was involved in fabrication of the thin film using drop-coating method. Toluene and hexane both could be used as the solvent of the ink to improve self-assembly. A line scan by TEM confirmed the composition of the thin film.

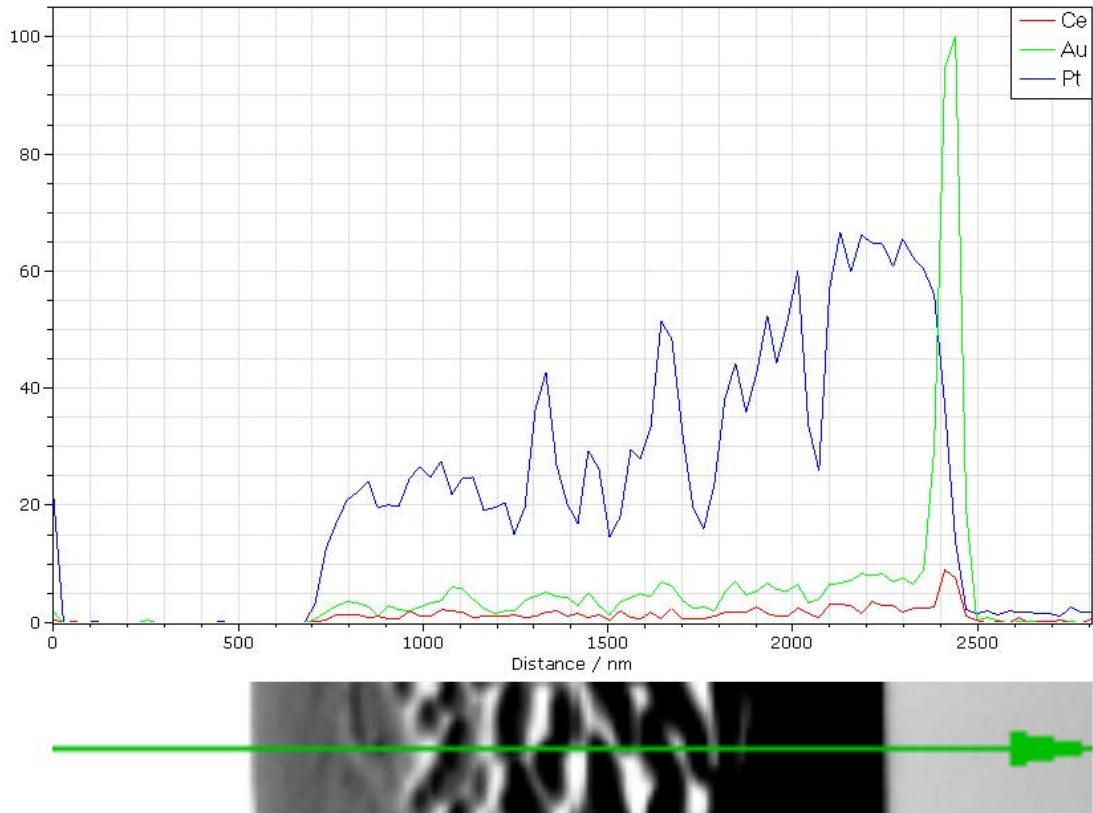
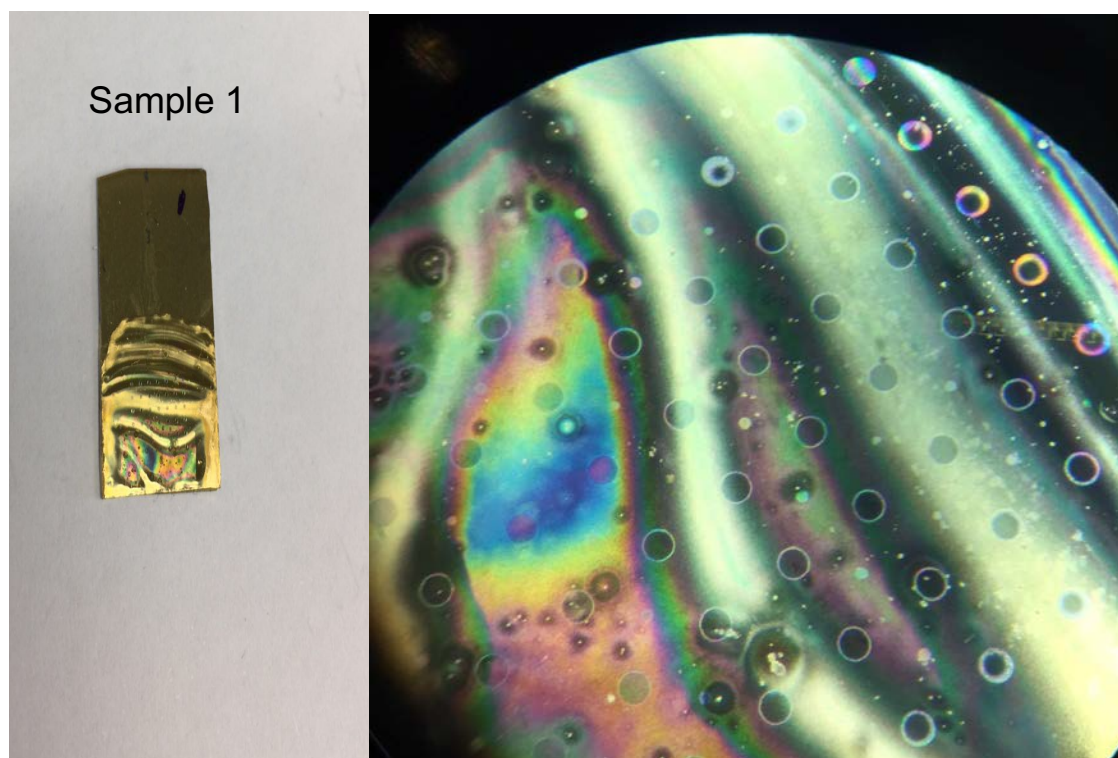


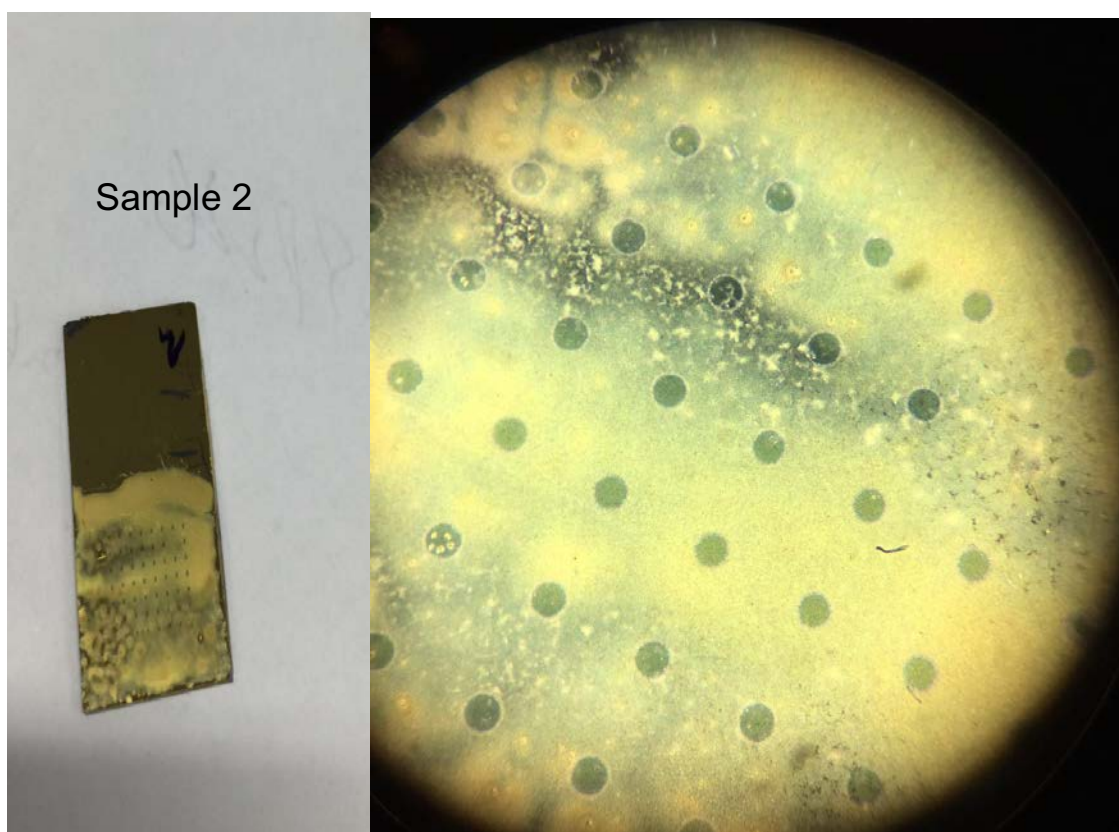
Figure 21. Line scan of thin film

The SEM test of both samples was done to compare the morphology of the thin film. Plasma processing technique has been significantly reduced top electrode drainage problems [112] from the sputtering process by producing a highly

dense , compact and cracking-free [113] CeO_2 thin films. Sample 1 used toluene as the solvent and other conditions were the same as that of sample 2.



*Figure 22. Sample 1: Hexane (0.5% oleic acid), plasma 1h (O_2) thin film
Sample 2: Toluene (0.5% oleic acid), plasma 1h (O_2) thin film*



There was nearly no crack in sample 1, and only some elongation and agglomeration occur in this sample. In sample 2, the agglomeration was more rapid. The boiling point of hexane and toluene was 69°C and 110.6 °C [114,115], respectively. Both of them were lower than the boiling point of OLA [114], 360 °C, so the agglomeration occurred in both sample.

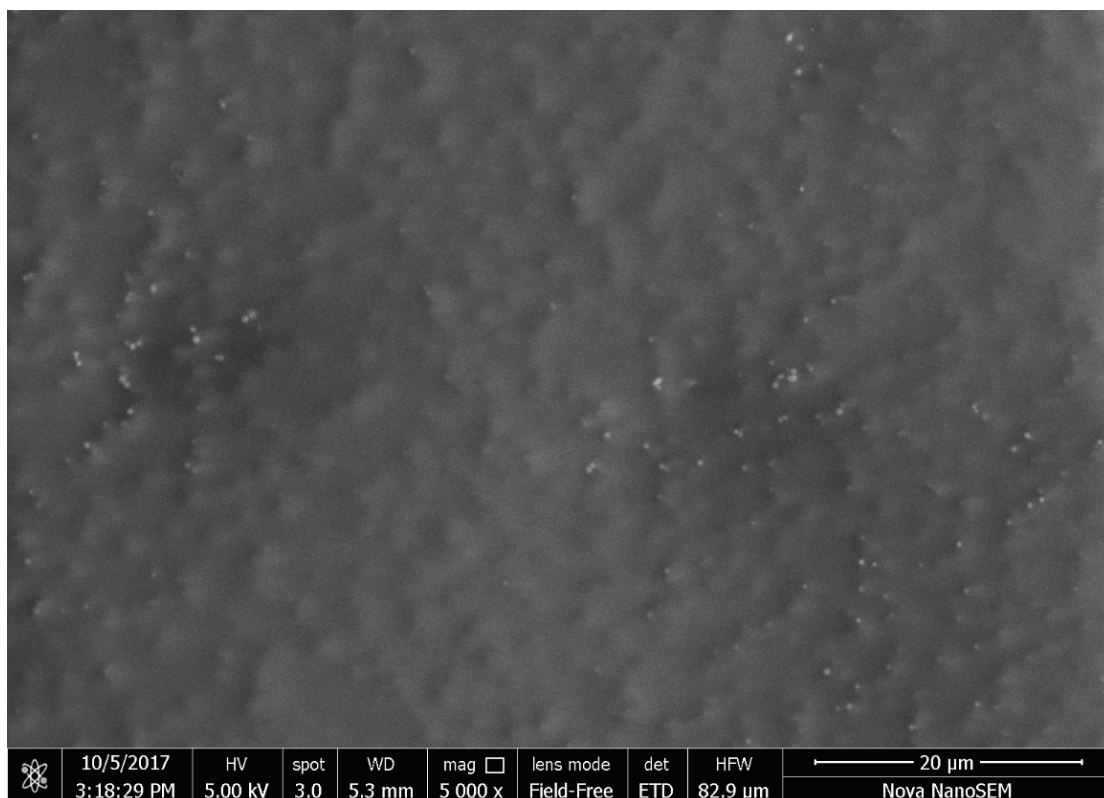


Figure 23. Morphology of Hexane (0.5% oleic acid), plasma 1h (O₂) thin film

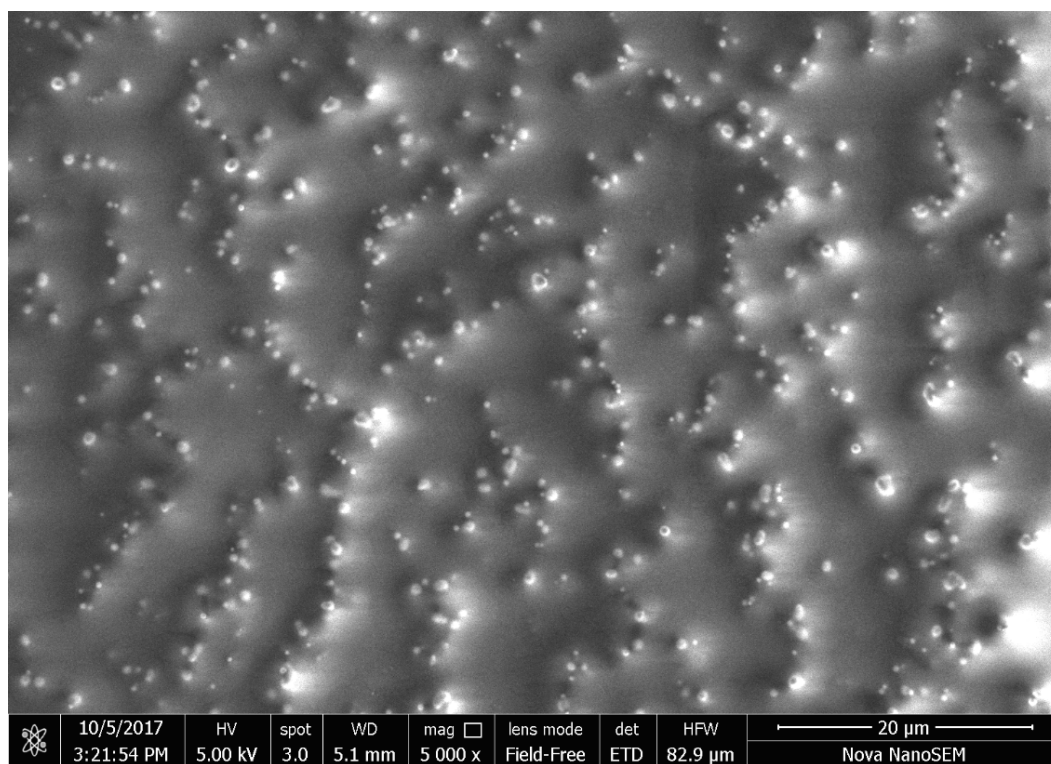


Figure 24. Morphology of Toluene (0.5% oleic acid), plasma 1h (O_2) thin film

Plasma processing technique could reduce top electrode drainage issue from the sputtering process by producing a highly dense, compact and cracking-free CeO_2 thin films. During the plasma treatment (high temperature dried out), the boiling point of toluene was higher than hexane and took the role of solvent for more time thus reduce the rate of agglomeration. OLA was hard to break down so the thickness of the thin film raised [116]. Sample with solvent of toluene had better resistance switching change than the one with hexane (Figure 25). Overall, the switching phenomenon was not critical for both samples, which can be ascribed as a cooperative action of the positively charged oxygen vacancies [117] and external electric field due to a thick switching layer [118].

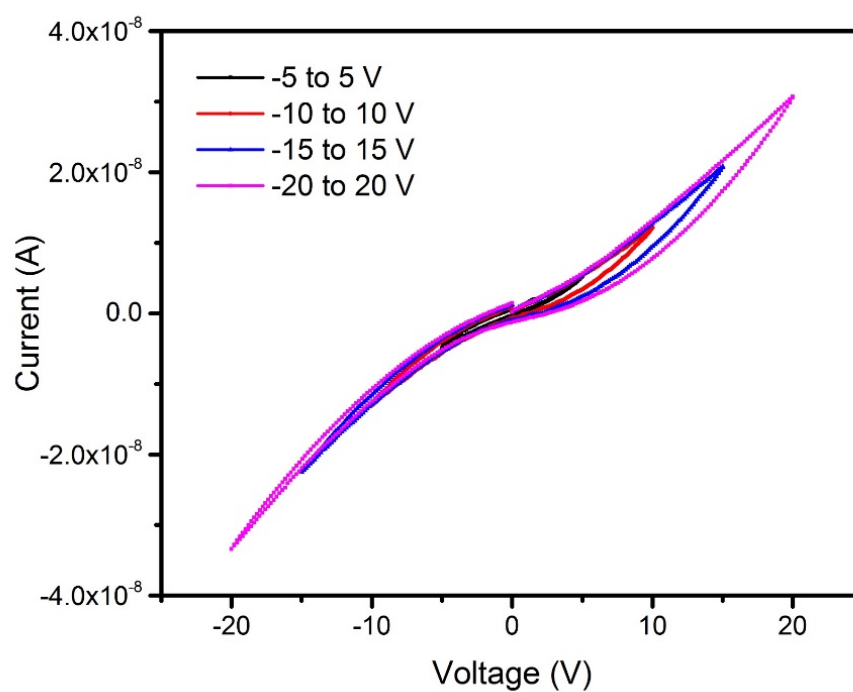
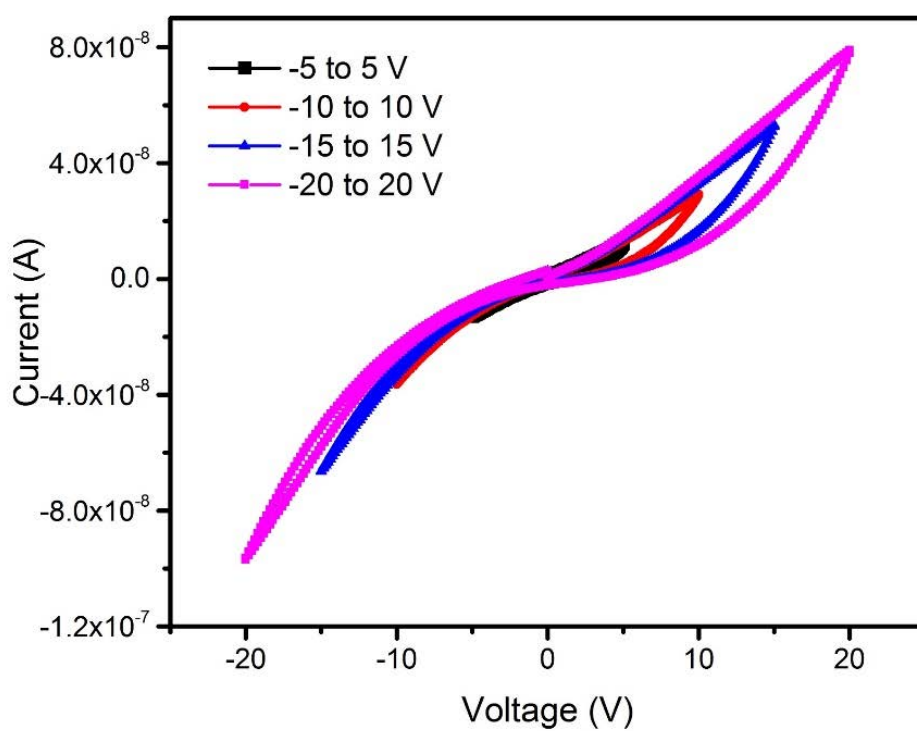


Figure 25. Resistance switching of (1) Toluene (0.5% oleic acid), plasma 1h (O_2) (2) Hexane (0.5% oleic acid), plasma 1h (O_2)

4.1.2 Effect of Plasma Treatment Time

Longer plasma treatment time can increase the break down ratio of OLA. The reduced rate of agglomeration would decrease the effective thickness of the switching layer so as to accomplish a stable bipolar resistance switching behaviour. Gold and Platinum were coated as the bottom electrode of the device. The thin films were done by drop-coating method follow by a 4 hour O₂ plasma treatment. The SEM figures were shown below.

Large cracking area had been found due to over drying of both samples. The percentage of agglomeration was a trade off with crack generation. Longer drying time do reduce the agglomeration but introduce the formation of crack on the surface of the thin film. There is no significant impact on surface morphology due to the bottom electrode.

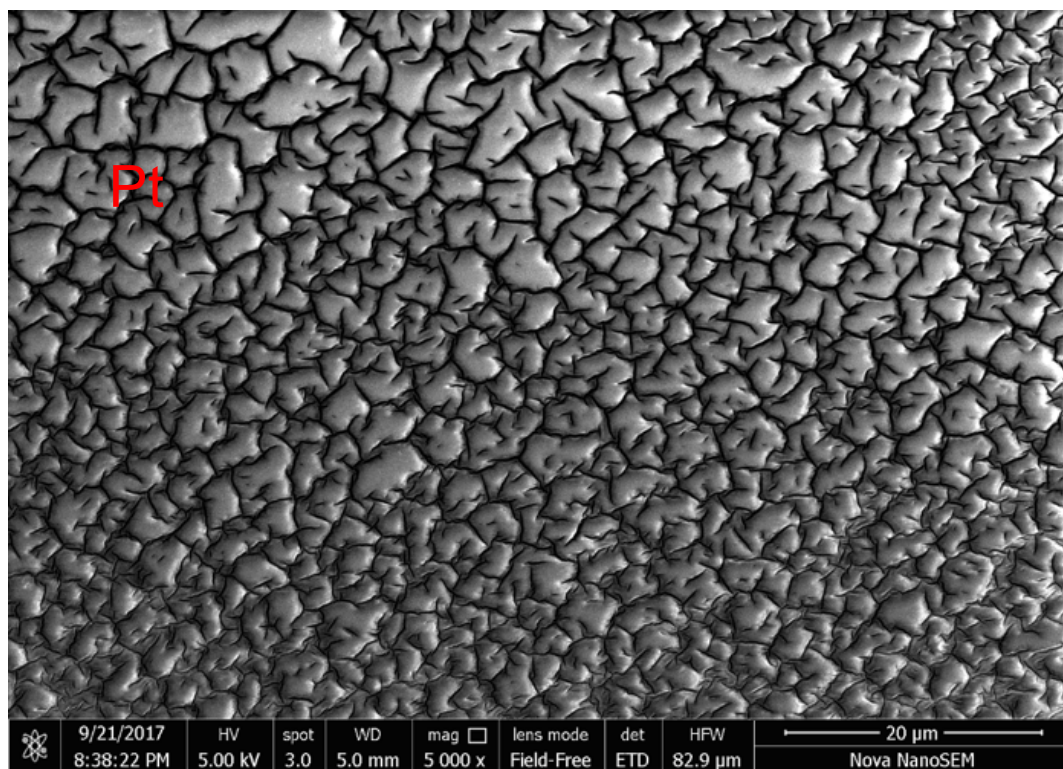
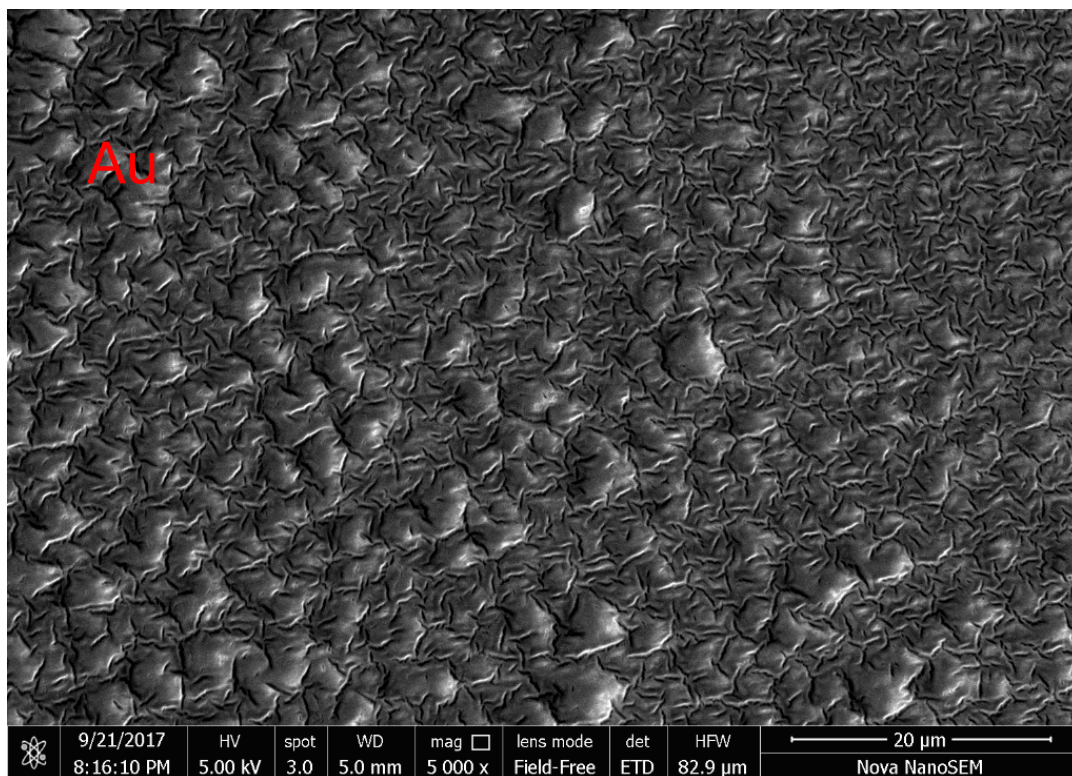
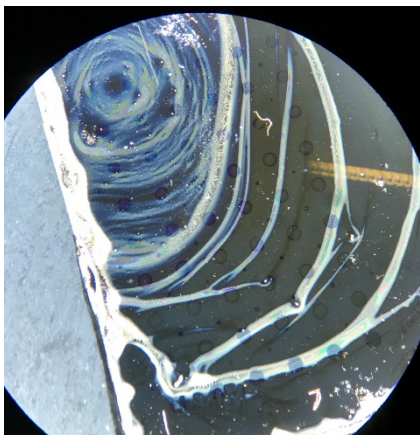
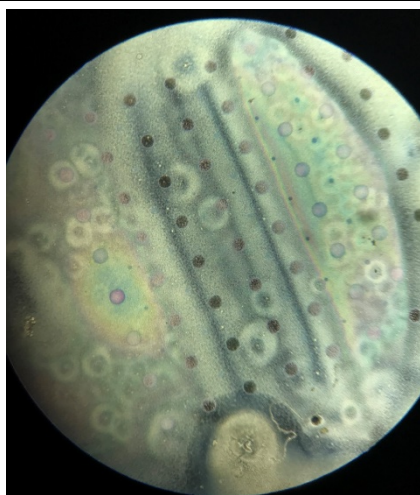


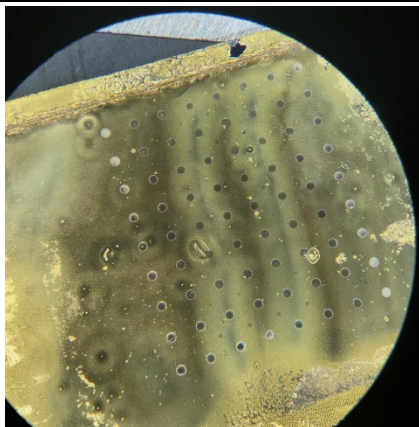
Figure 26. Morphology of Toluene (0.5% oleic acid), plasma 4h (O_2) thin film
 (1) Gold coated substrate (2) Platinum coated substrate

4.2 Electrical Properties of Thin Film Device

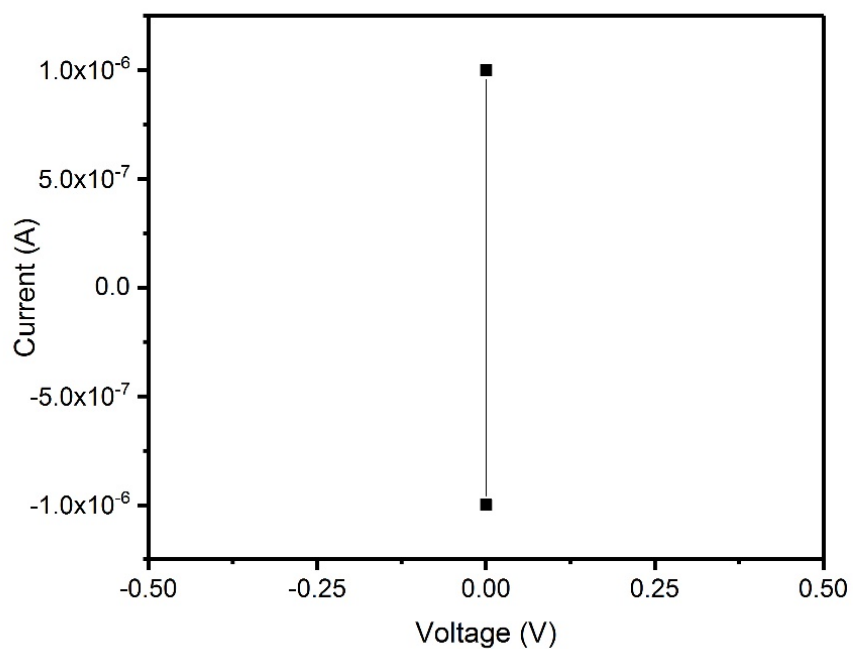
Three samples were made to compare the thickness of the thin film and improved the resistance switching phenomenon. Table below listed the determinant factors of each sample. The samples were made by spin coating method.

Table 5. Determinant factors for sample 1-3

	Solvent	Thickness	Surface of samples
Sample 1	Pure Toluene	1 layer	
Sample 2	Toluene with 0.5% oleic acid	1 layer	

Sample 3	Toluene with 0.5% oleic acid	3 layers	
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The surface of sample 1 had obvious defect due to lack of self-assembly for the nanocube in the ink. Sample 2 and sample 3 were crack free and the switching phenomenon was test for all three samples.



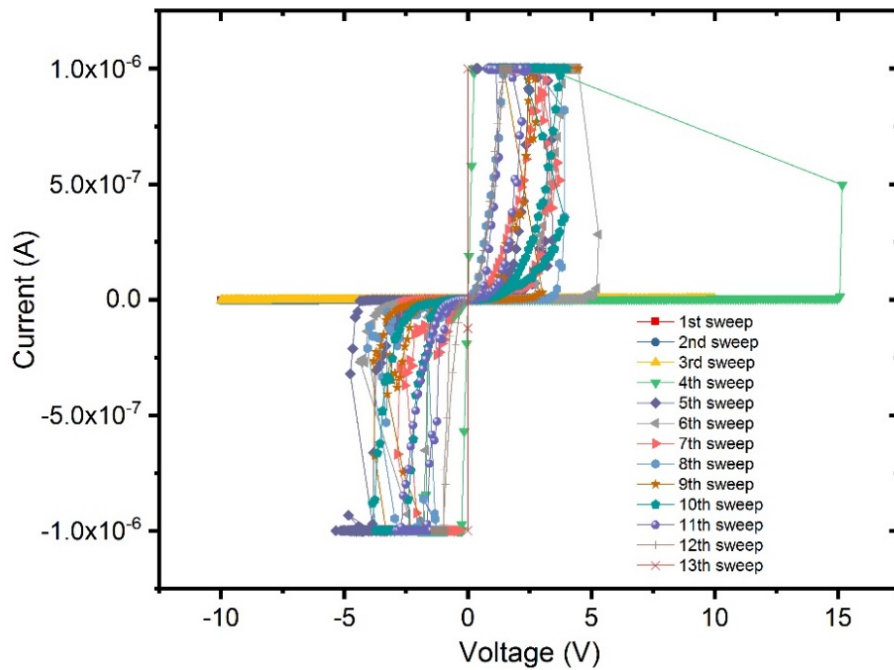
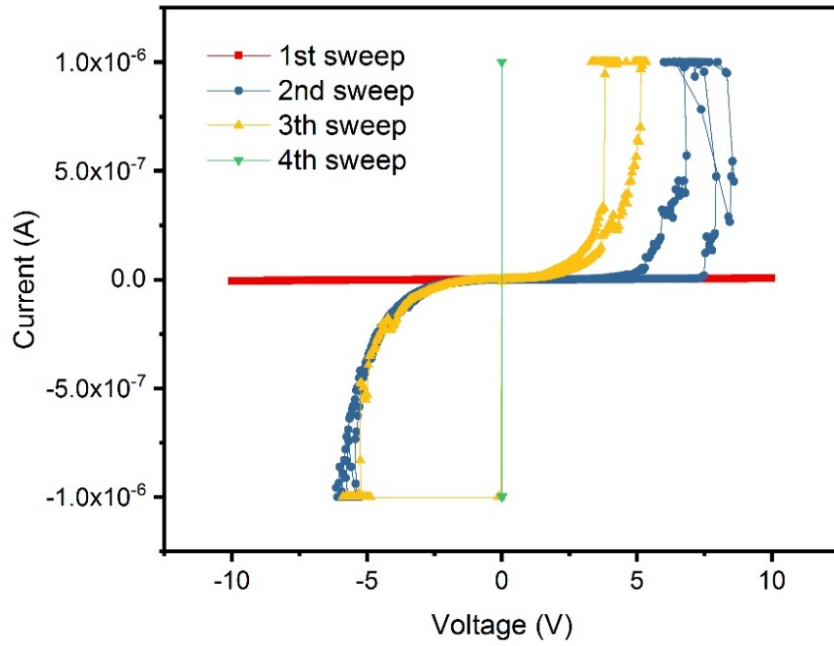


Figure 27. Best I-V curve for Sample 1, Sample 2, Sample 3 (top to bottom)

For each sample, 5 different points of electrode had been chosen for each trial. No resistance switching behaviour had been found in sample 1. Unstable

switching with less sweep had been found for sample 2. Most sweeps and relatively stable resistance switching occurred in sample 3. The result confirmed that the self-assembly [119] of the nanocubes in suspension ink could influence the morphology and electrical properties of the thin film devices. A reasonable thickness of the thin film was required to ensure the resistance change and the endurance of the device. The resistance change was mainly caused by moving of oxygen vacancy [120]. Plasma treatment improves the activity of the vacancy transportation, and the reasonable thickness of the thin film ensured the transportation to take place. Both factors resulted a better evident resistance switching phenomenon in sample 3.

4.2.1 Improve by Adding Organic Ligands

Recent researches have been raised the relationship of stress and crack generation [121-124]. The bottom-up approach was employed to reduce the crack produced during the densification of the nanocubes into a solid-state thin film. Stress could overcome weak forces and hold colloidal nanoparticles together. The ordered colloidal nanoparticles had more chance to cause a cracking surface [125] especially when removing the ligands (the carbon concentration was decreased to 0.6% through plasma treatment). An organic ligand calibration was then employed to improve the CeO₂ ink.

The organic ligand [126] used in this experiment was trioctylphosphine oxide (TOPO), a polar molecule ligand calibration. The close-packed TOPO molecules could bond to the same surface due to the phosphine oxide group

and suffer a dipole-dipole interaction, thus the molecules would repel with each other. The poor solvation of TOPO ligand shell could result in a formation of 'sticky' surfaces of building blocks which can obstruct a 3D ordered assembly by yielding kinetically trapped nanocubes. The poor solvation also caused an interdigitation with potentially yield more cohesive array of molecules so as to achieve a compact, dense, non-cracking, porosity-free thin film and ensure a reproducible electrical property [125,126].

TOPO was added at the ratio of 0.13g/1ml in both toluene and hexane based CeO_2 suspension solution. Thin film deposition was conducted by drop coating and spin coating. The samples were then going through a drying process under the O_2 plasma treatment for 5 hours.

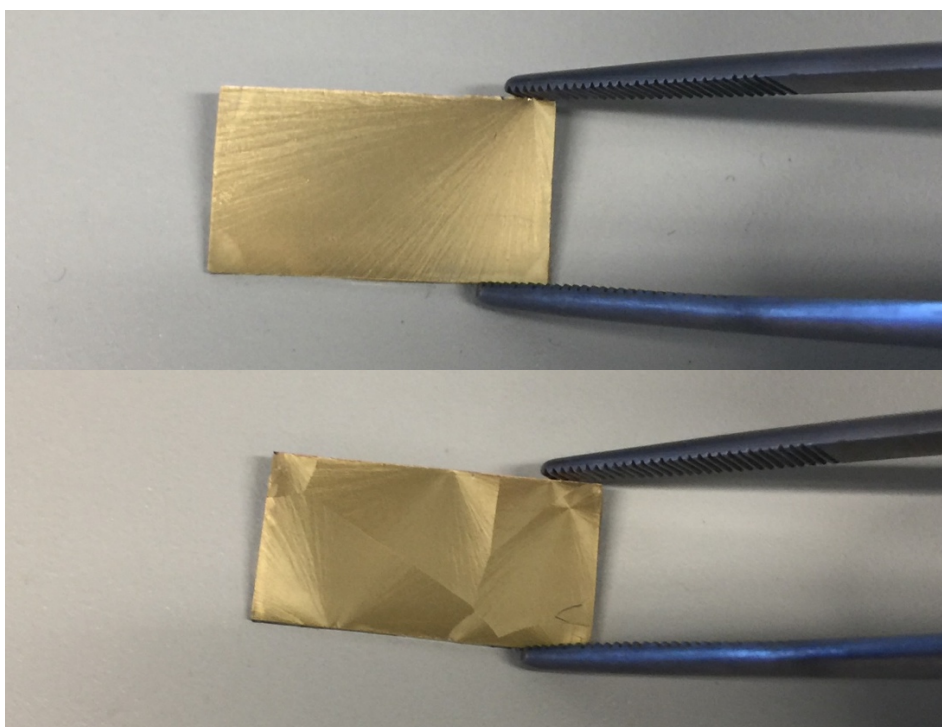
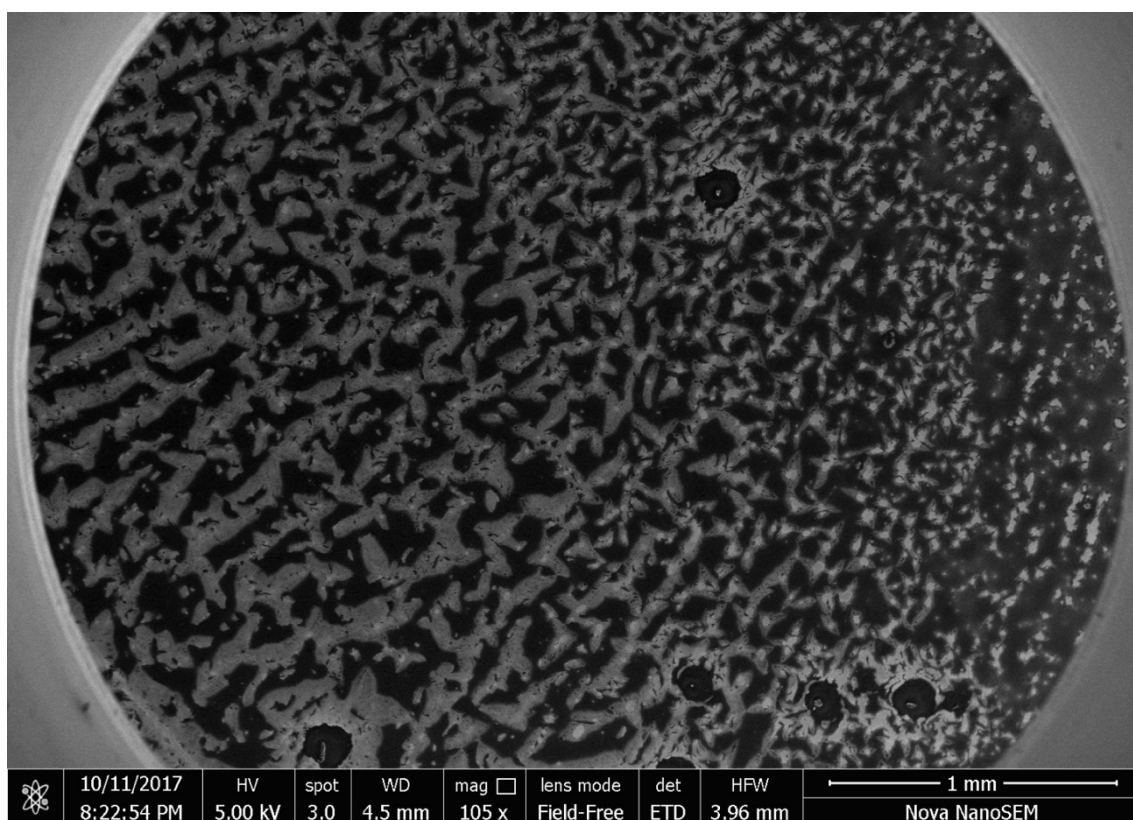


Figure 28. (1) Toluene with TOPO (2) Hexane with TOPO on Au coated Si substrate

It was seen that 5 hours were not enough to completely remove the ligand; extra hours of plasma treatment were necessary to be taken. As spin coating deposition produces comparable thinner films, SEM examination was only carried out on the spin-coated samples after 5 hours' plasma treatment. The result thin films of drop coating were too thick that could hardly be observed with SEM.

Figure 29 (1) and (2) were relative darker than normal SEM images, indicated a non-drying thin film and the black regions shown the part of wet solution. Longer treatment time would result increasing chance of crack producing. TOPO was hard to be decomposed and create an organic compound layer on top of the thin film thus reduce the detection of the electrical properties of the thin film.



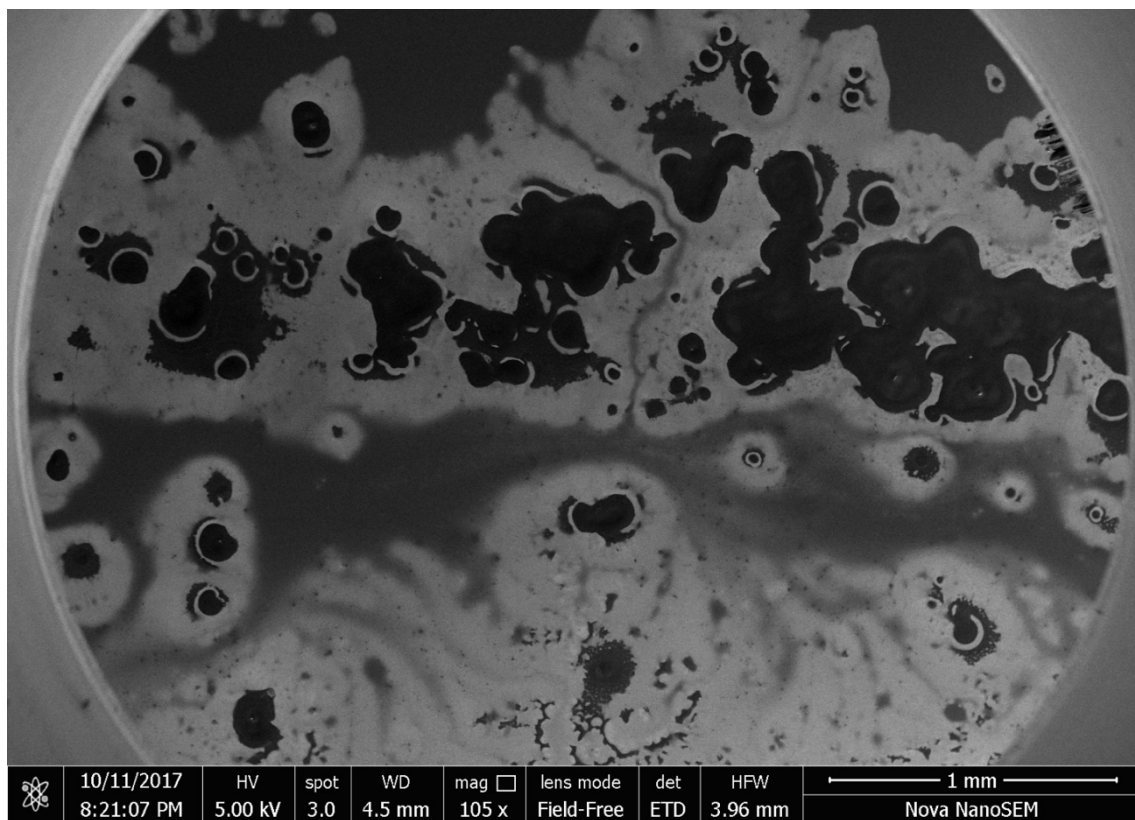
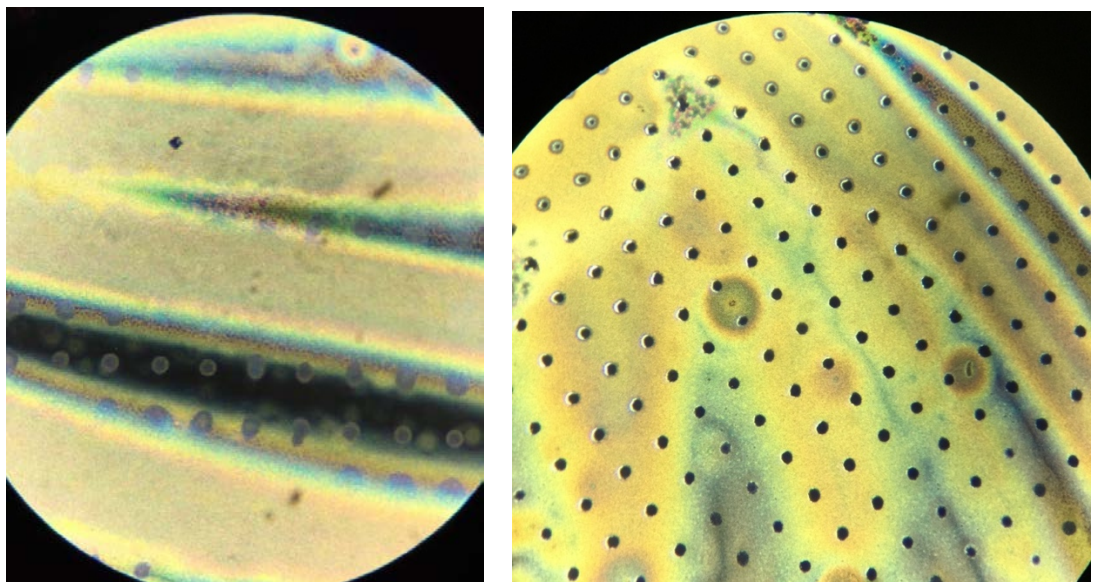


Figure 29. SEM images of spin coated (1) Toluene with TOPO (2) Hexane with TOPO on Au coated Si substrate after 5 hour O_2 plasma

4.2.2 Inkjet Printing of Top electrode deposition

One of most effective defect of the device which compromise the performance of the electrical properties of the device was that top electrode drainage during sputtering process. Inkjet printing for top electrode deposition promises contact-free processing environment (especially, no physical scratches or damage on the thin film produces during the processing), it also allows a more accurate and compact parameter alignment and customizable production size.

Instead of gold top electrode, a silver top electrode was used for inkjet printing process. The homogeneous conductive silver printing ink (35 wt% with 150 nm particle size) with fixed droplets size and space (250 μm) dropped on the cerium oxide films for two and five repeated times. The top electrodes were not clear to seen in sample 1 whereas in sample 2 the silver top electrode could be clearly verified.



*Figure 30. Sample 1: Inkjet printed for 2 repeated cycles (left)
Sample 2: Inkjet printed for 5 repeated cycles (right)*

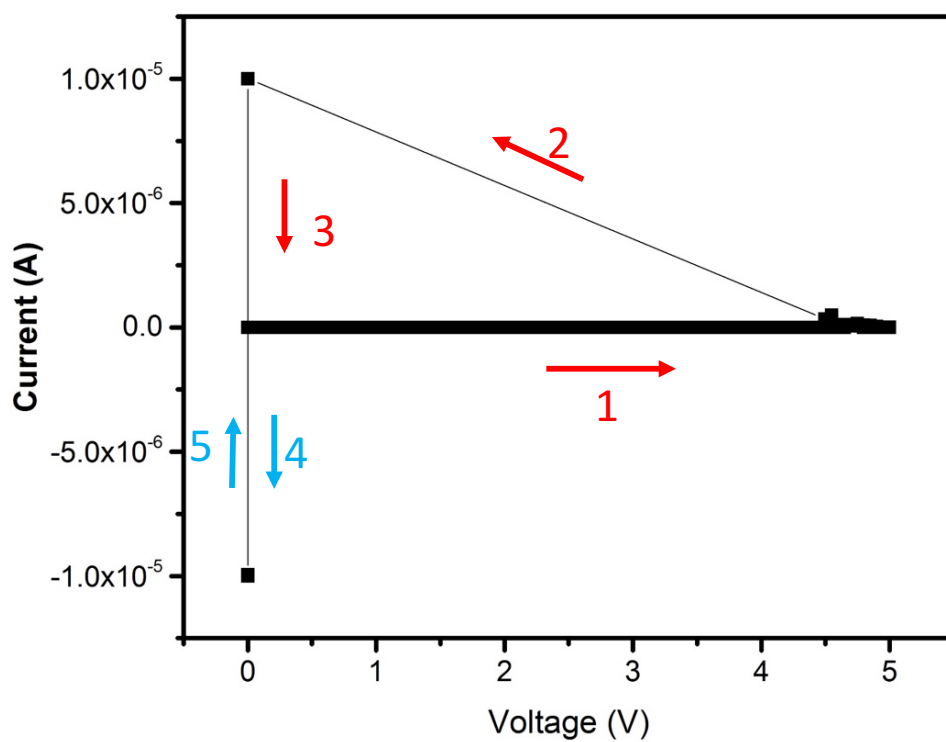
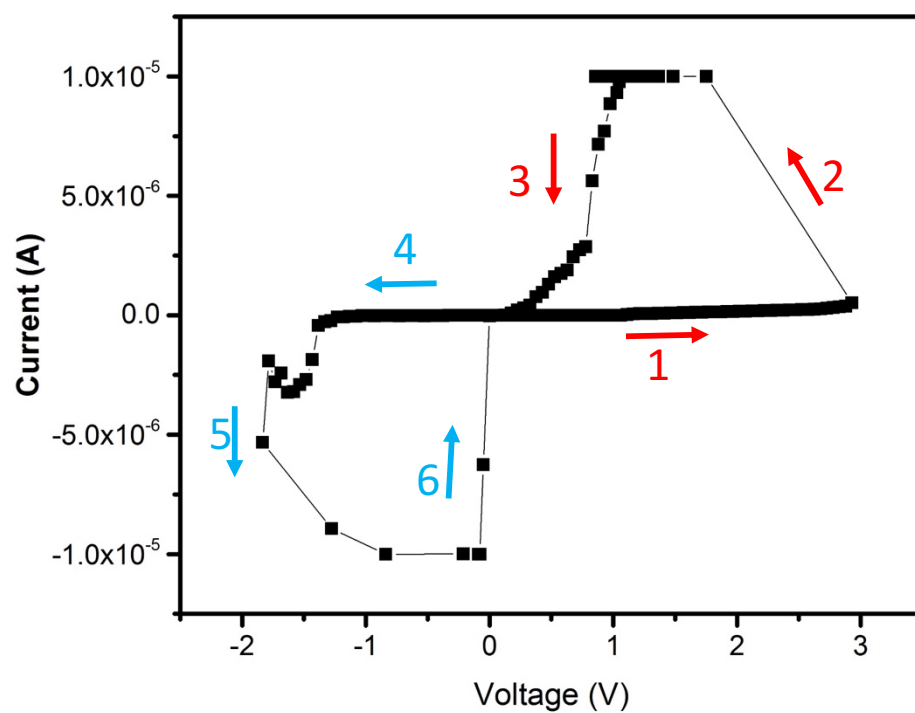


Figure 31. I-V curve for top electrode with (1) 2 repeated cycles (2) 5 repeated cycles

Plasma treated cerium oxide films have successfully demonstrated resistive switching behaviour by employing silver top electrode through a facile inkjet printing approach. The appeal of electrical properties also confirmed the inherent resistance change of the prepared CeO_2 thin films. The divergent resistive switching behaviour observed in both samples were based on the difference in silver quantity of the top electrode. The unipolar phenomenon was obtained when the amount of silver is deficient (more obvious in 5 repeated cycles of the silver top electrode).

5. TPU BASED CERIUM OXIDE THIN FILM DEVICE

Thermoplastic polyurethane (TPU) was an elastomer, which had typical properties of high elasticity, high shear strength and high abrasion resistance [127]. TPU was transparency [128], so the cracking could be indicated more easily. In conclusion, TPU was selected as the substrate for the stretching substrate of the thin film device. The substrates were cleaned using an ultrasonic cleaner. TPU was sensitive to high temperature performance and underwent thermal deformation after long time UV lightening. A short time of surface clean process was chosen. Silver was coated by a sputter to work as the bottom electrode for the device. The sample was a two-layers device with CeO_2 layer at bottom and 5% In-doped CeO_2 at top. For both layers, only one drop with 20 μmL ink was coated by drop-coating method. The sample was also covered by a gold top electrode under a similar method to silicon based samples. The original sample was made at an original length of 4 cm. The device was then stucked on a metal plate for I-V measurement.



Figure 32. Illustration of the TPU based device

The elongation was 1 mm for the stretchable state along the direction indicated by the red arrow. The strain was estimated by $\Delta L/L$, where L is the original length, ΔL is the length of elongation. The device was subsequently measured for five 'stretch-relax' cycles. Electrical properties were tested during each stage of the sample.

5.1 Surface Morphology

The sample was made using a spin coating method to improve the uniformity of the thin film. The TPU substrate was fixed on a piece of glass for spin coating to minimize twist.

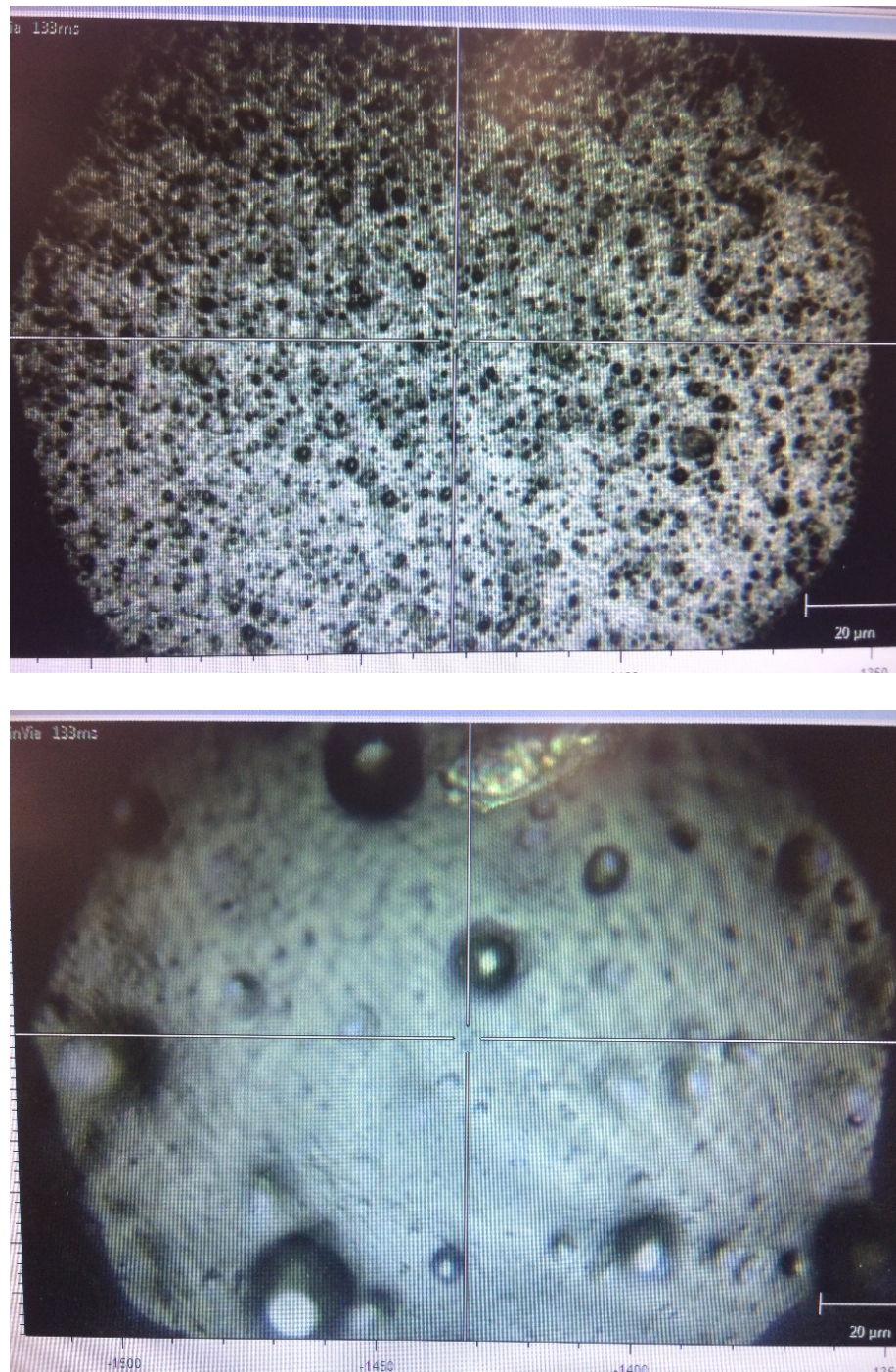


Figure 33. Morphology of TPU substrate



Figure 34. Morphology of CeO₂/In-doped CeO₂ thin film

From Figure 33, the surface morphology of TPU is porous. The ink could be permeated into the TPU substrate. Furthermore, TPU is not as reflective as silicon or other conductive glass substrate with gold bottom electrode, it was difficult to tell whether the OLA was completely removed from the thin film or not. SEM was not sufficient to analyse the surface structure in this case. A FIB test was done to analyze the thin film more closely.

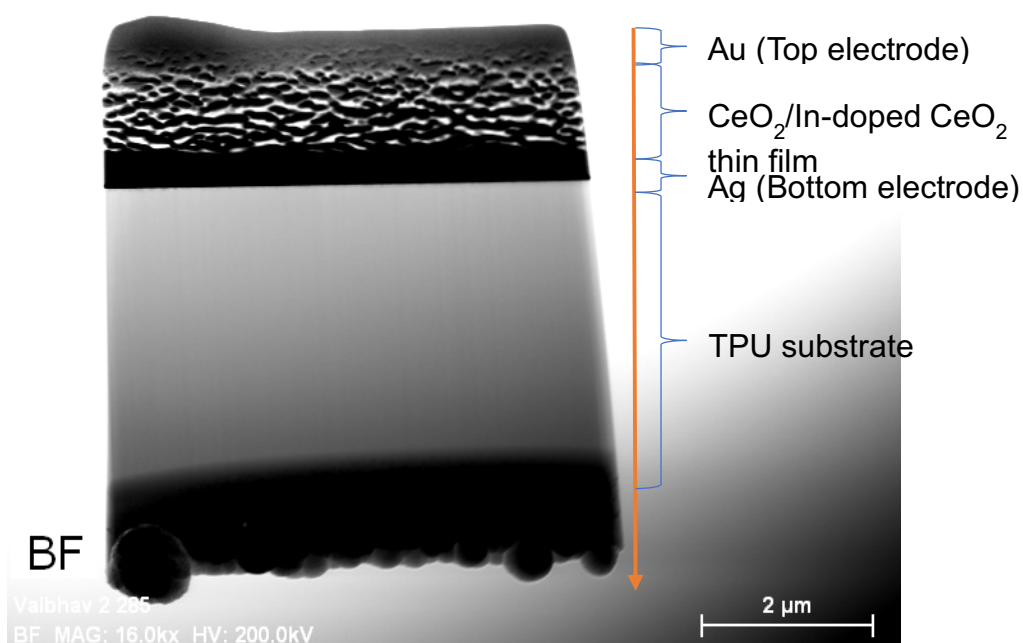


Figure 35. FIB of CeO₂/In-doped CeO₂ Device

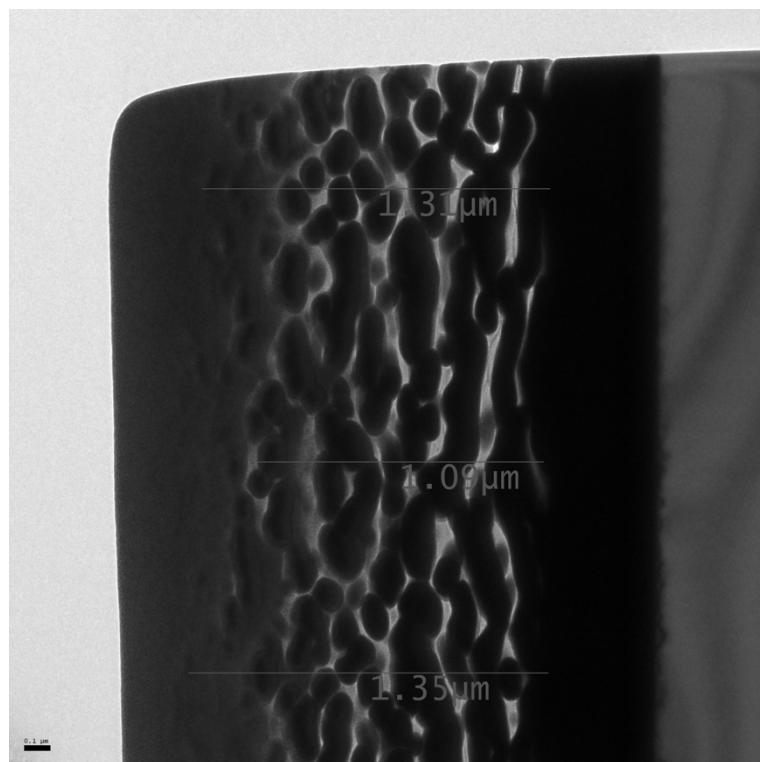
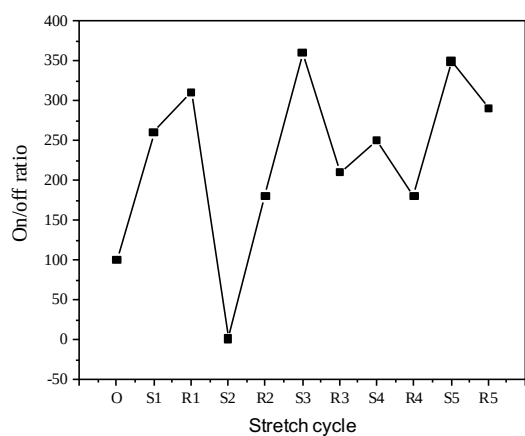


Figure 36. Thickness and morphology of CeO₂/In-doped CeO₂ thin film

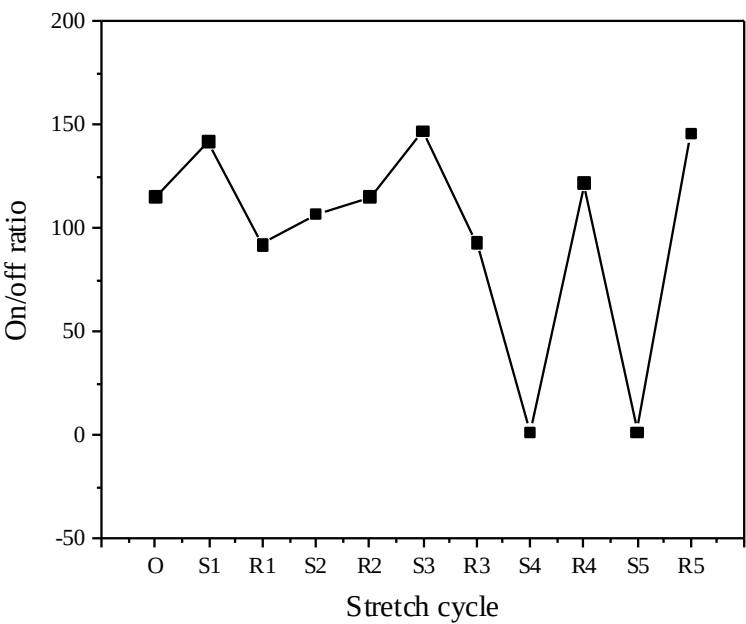
The composition of the thin film layers was indicated on Figure 35. The thickness of the thin film was around 1.32 μm. There exist some elliptic shaped conglomeration [127] in the thin film. Therefore, another problem was that the ink dried much more quickly than that on the other substrates. Solvent diffused more quickly and conglomeration occurred easily.

5.2 Stretching Test with On/off Ratio

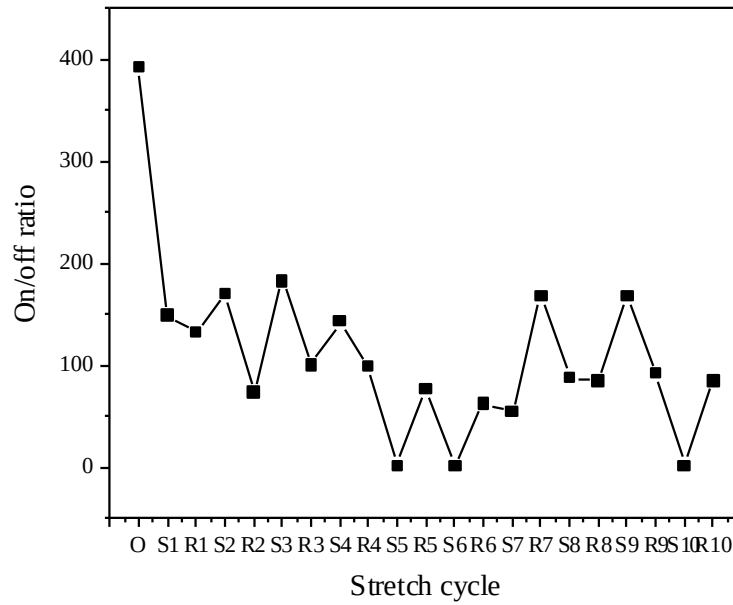
Three samples were tested with a length of elongation of 1mm, 2mm, 4mm, respectively. (Figure 37) The corresponding strains were 2.5%, 5%, and 10%. The on/off ratio for each state (original state - O, stretch state - S, and relax state - R) in 'stretch-relax' cycles were recorded blow.



Sample A: $\Delta L = 1\text{mm}$, Strain: 2.5%



Sample B: $\Delta L = 2\text{mm}$, Strain: 5%



Sample C: $\Delta L = 4\text{mm}$, Strain: 10%

Figure 37. On/off ratio for each state (original state - O, stretch state - S, and relax state - R) in 'stretch-relax' cycles: Sample A-C

The resistive switching behaviour can be observed even after 5 cycles. However, no typical regularity could be attained. This was because TPU has poor thermal conductivity, thus a silver conductive coating was required. Cracks generated while stretching, which gave rise to short circuit in some areas. Nevertheless, it still worked at another point. In addition, the measurement points burned straight frequently after the stretching test shown that the heat generated during the test had not been released and reduce the performance of the device. The CeO_2 suspension ink with a solvent of toluene had chemical reaction with the TPU [127] and arise the problem of substrate shape change. Moreover, the CeO_2 ink flowed in an uncontrollable direction and influenced the uniformity of the thin film layer result an unstable on/off ratio for the devices.

5.3 Electrical Properties of Devices

A device with TPU substrate, with the structure of Au/CeO₂/Au/TPU, was tested for the electrical performance. A length of elongation of 1mm was chosen for stretching testing. Voltage – current sweeping and endurance test were conducted for the device in original state, stretching and relaxing state, respectively. The resistance change existed in the sample but which is not stable, and the sample was damaged after testing. Different points on the same sample would result similar voltage change thus double confirmed the electrical properties of the thin film. Resistance change for one cycle was called a 'stretch-relax' (Original state -> Stretching state -> Relax state) cycle. Typical I-V curves and endurance test of each state are shown below.

Figure 38 (a) shows the I-V curves of the TPU device, where resistive switching can be found. However, the device has a small ON/OFF window around 5, as shown in Figure 38 (b). On the other hand, there are some noises in the endurance curve, which may be caused by the stretchable nature of TPU. The resistive switching behaviour of the device was also tested under stretching state. As shown in Figure 39 (a), the I-V curves became unstable and the ON/OFF ratio was only around 3. It is interesting that the device is more stable compared with original state, as indicated in Figure 39 (b). After relaxing, the device shows similar resistive switching with original one, which are shown in Figure 40.

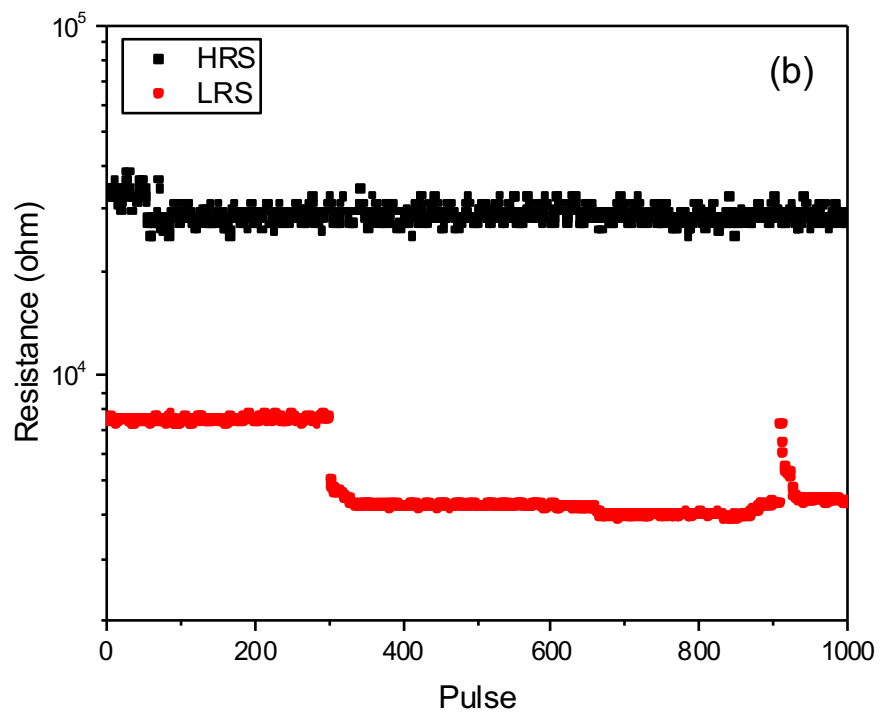
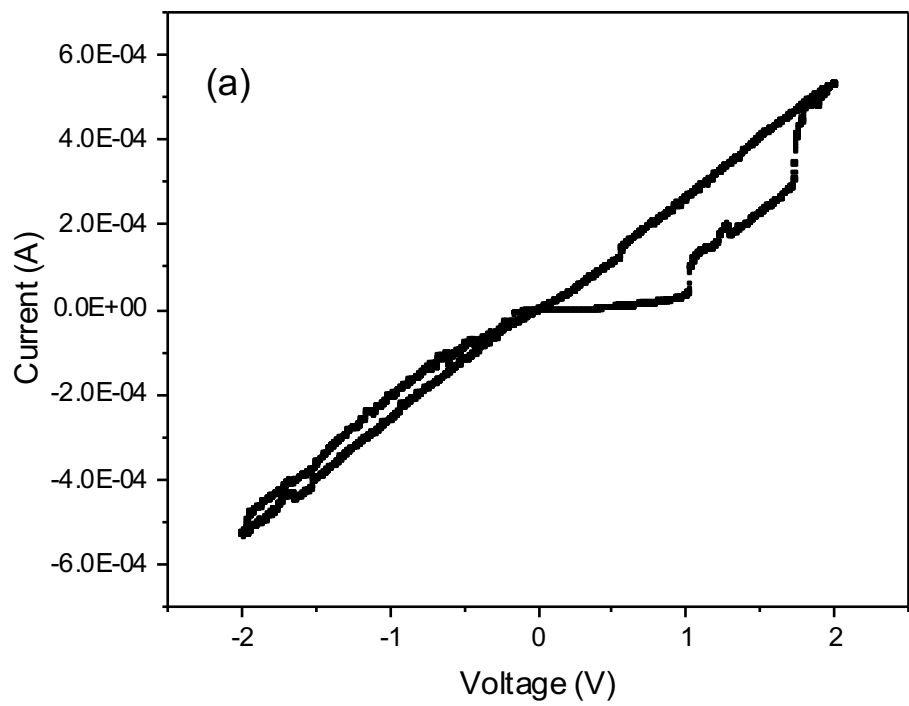


Figure 38. Original State: (a) I-V curves (b) Pulse change

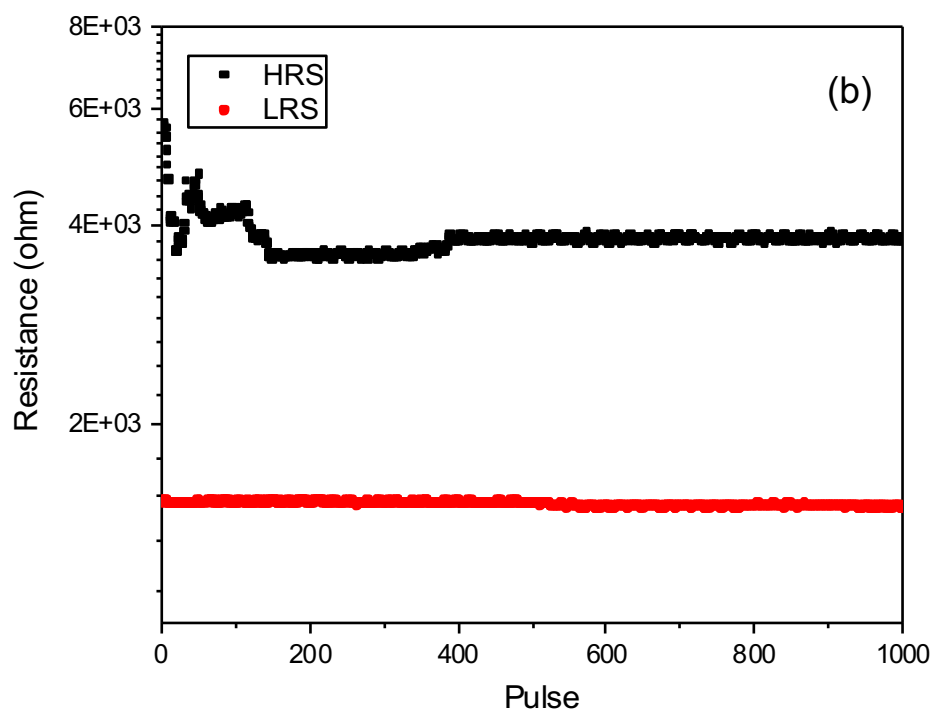
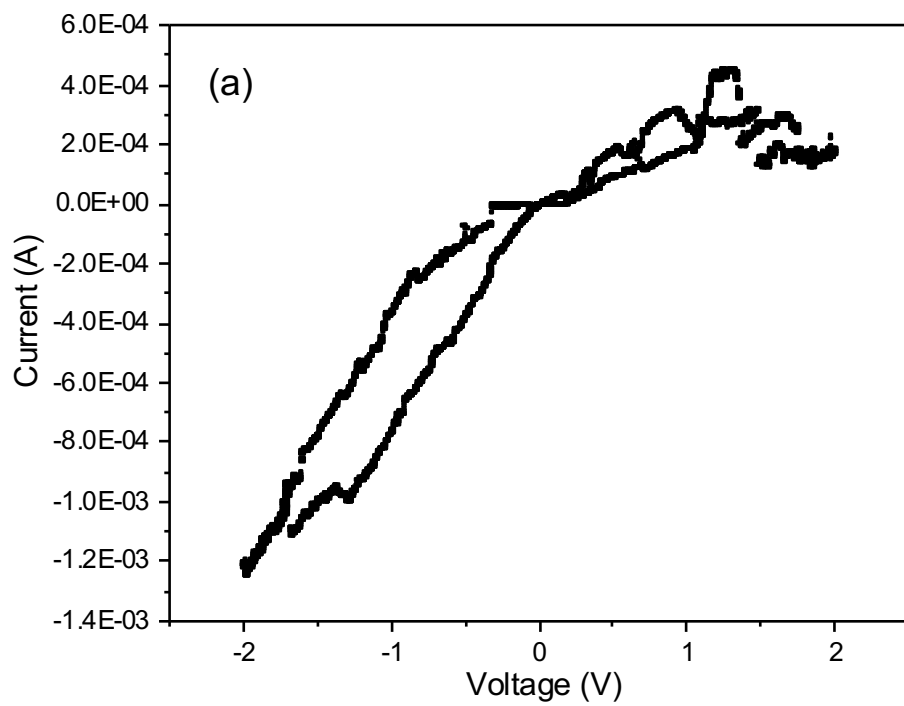


Figure 39. Stretching State: (a) I-V curves (b) Pulse change

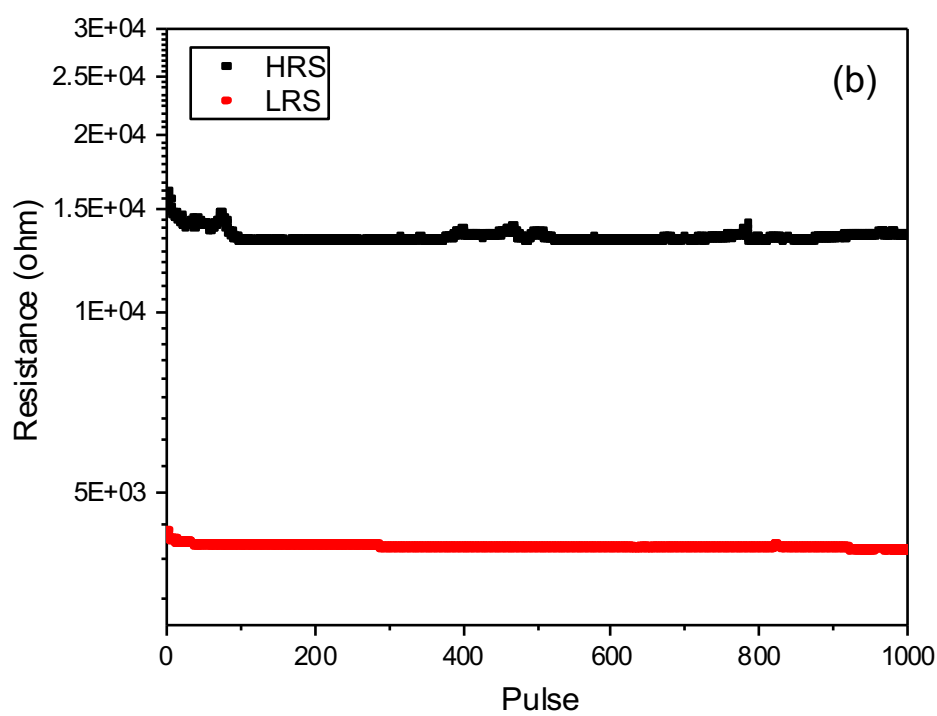
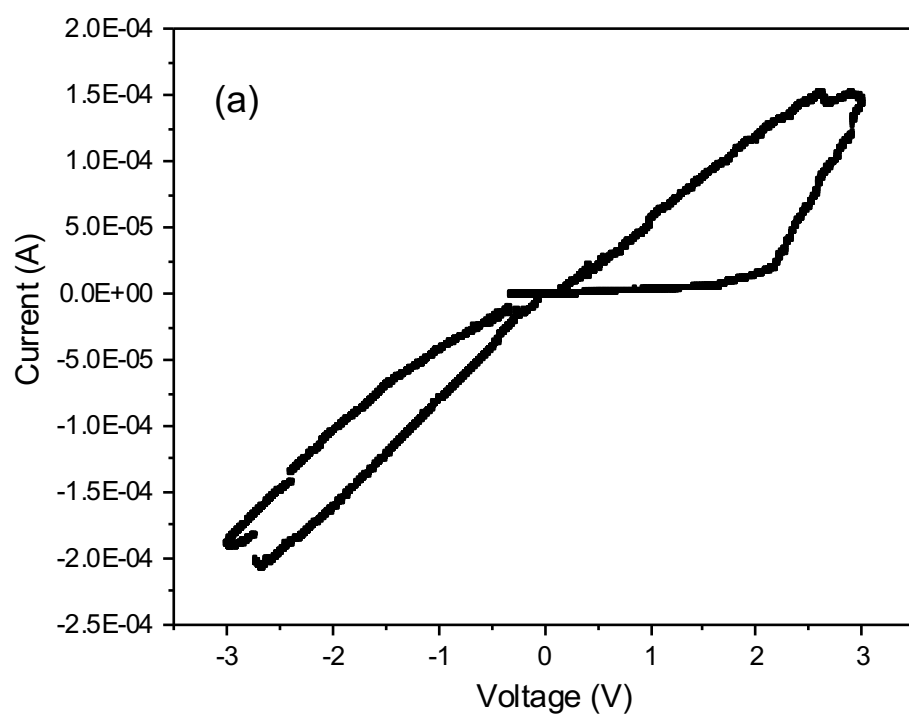


Figure 40. Relaxing State: (a) I-V curves (b) Pulse change

For a successful point the resistance change should occurs in all three states (Cycle 1,2,3) and passing the 1000 times endurance test as well. Moreover, a sample with several points (points were numbered using a matrix) were tested for pristine state and same testing process after 100 cycles of stretching. The results were shown in the following tables. For each symbol in the table, a typical sample of resistance change were given below.

- refers to the fixed top electrode.
- X in the table indicates failure within the first 3 times I-V sweeps.

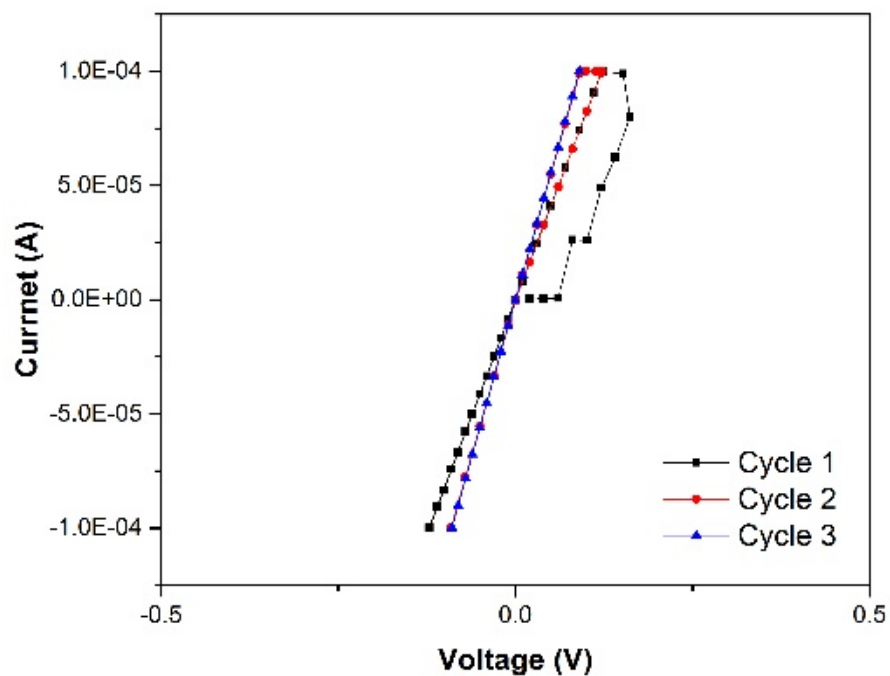


Figure 41. Typical I-V curve for failure within first 3 times I-V sweeps

- X with yellow highlighted in the table indicates the point exist a resistance change but failed during the 1000 times endurance test.

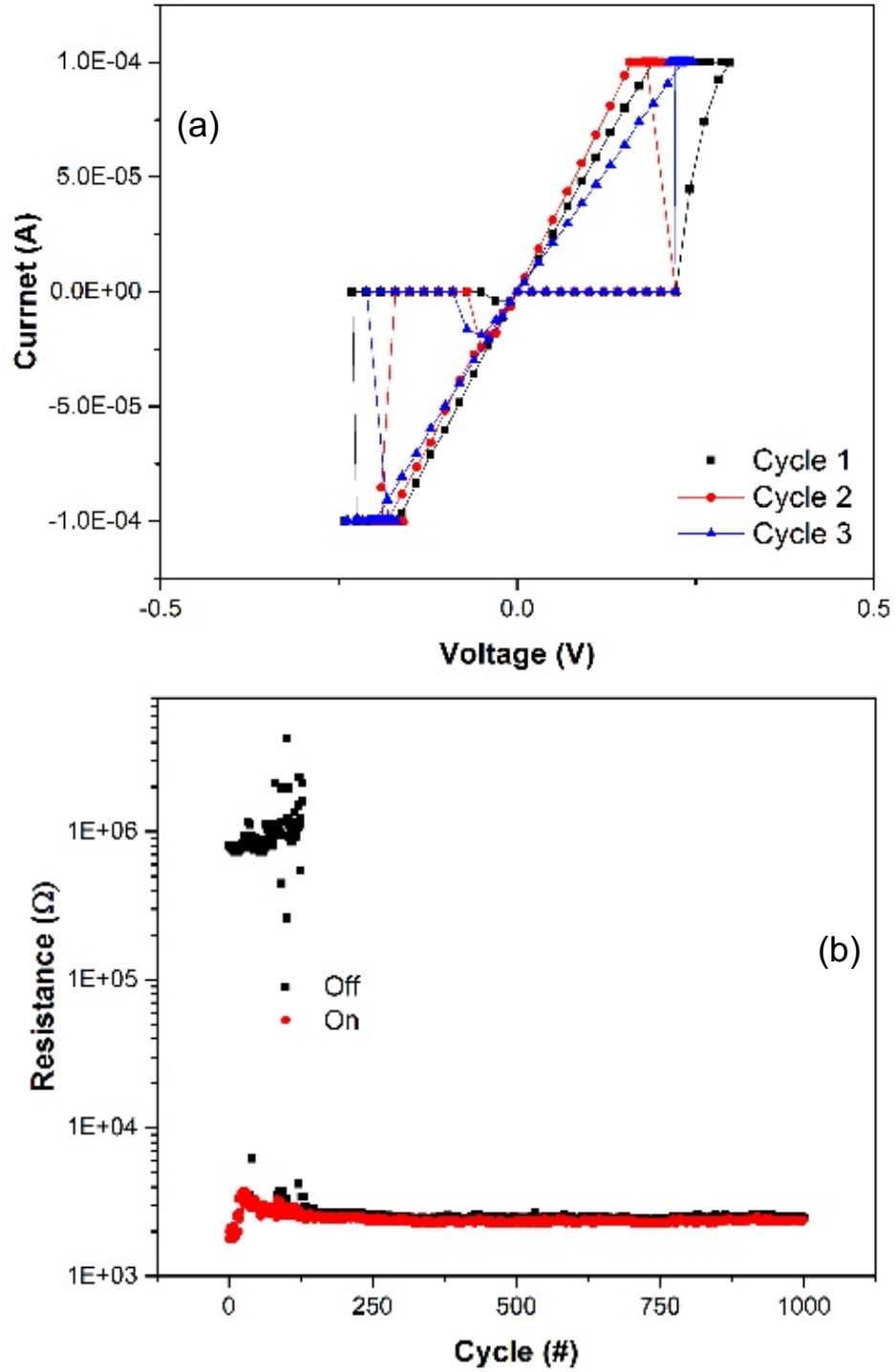


Figure 42. Typical (a) I-V curve and (b) endurance change for successful resistance change but failed during the 1000 times endurance test

- $\checkmark$ with green highlighted in the table indicates a test of point was success.

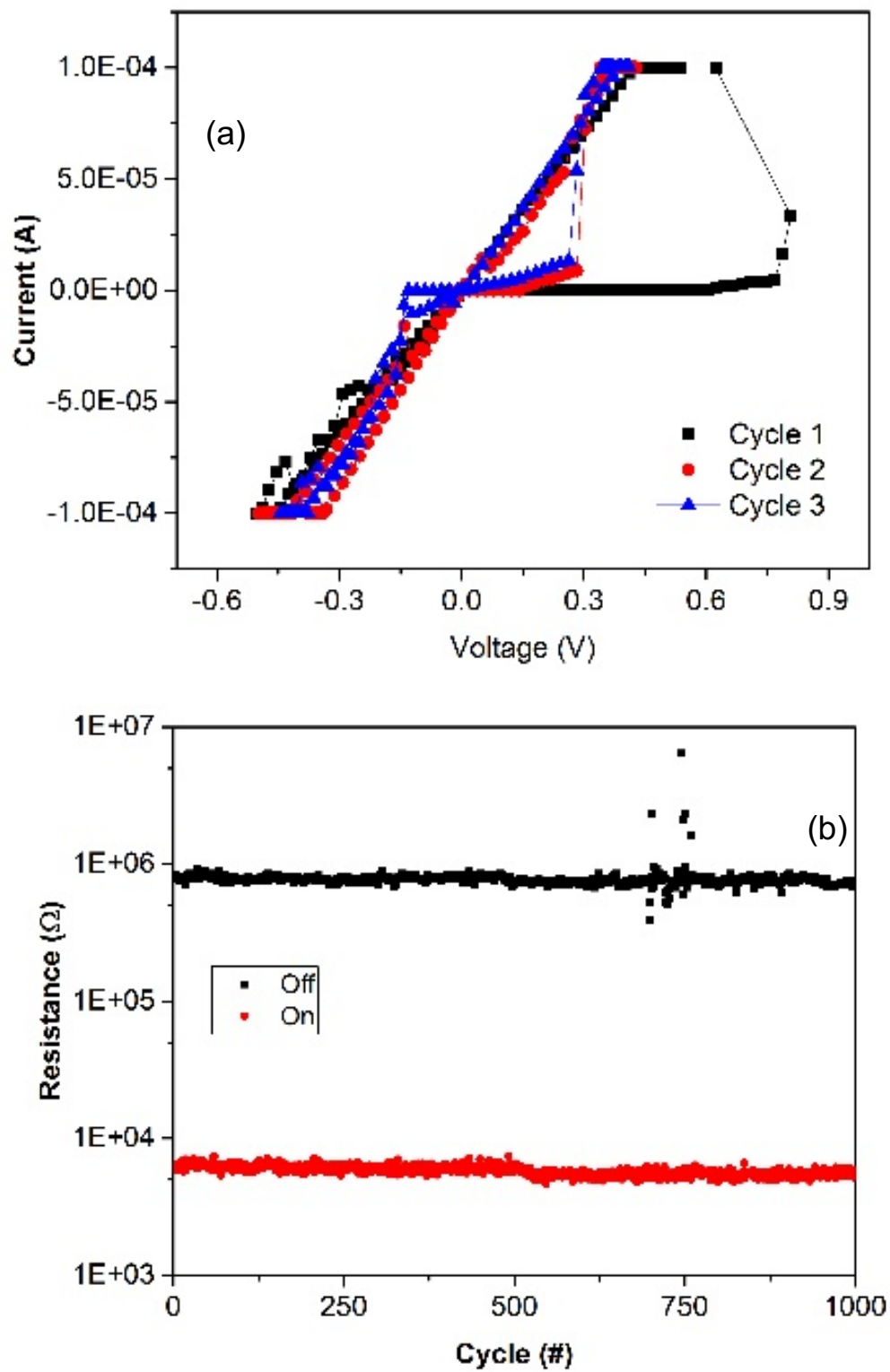


Figure 43. Typical (a) I-V curve and (b) endurance change for successful resistance change and 1000 times endurance test

Table 6. Device performance matrix at pristine state

	A	B	C	D	E	F	G	H	I
1	√	X	X	X	X	X	√	√	√
2	X	*	X	X	*	X	√	*	√
3	X	√	X	X	X	X	X	√	√
4	√	X	√	X	X	X	√	X	X
5	X	*	X	X	*	X	√	*	√
6	√	X	√	X	X	X	√	X	√
7	X	X	X	X	X	X	√	√	√
8	X	*	X	X	*	X	√	*	X
9	X	X	X	X	X	X	√	X	√

Table 7. Device performance matrix after 100 cycles of stretching

	A	B	C	D	E	F	G	H	I
1	X	X	X	X	X	X	X	√	X
2	X	*	X	X	*	X	X	*	√
3	X	X	X	X	X	X	X	X	√
4	X	X	X	X	X	X	X	√	X
5	X	*	X	X	*	X	√	*	X
6	X	X	X	X	X	X	X	X	√
7	X	X	X	X	X	X	X	X	√
8	X	*	X	X	*	X	√	*	X
9	X	X	X	X	X	X	X	X	√

On the basis of the two tables above, the success rate of device performance matrix at pristine state was 24/81 (√ with green highlighted: nearly 29.63%).

This rate was rapidly decreased after 100 cycles of stretching, the successful test was 9/81 (√ with green highlighted: nearly 11.11%). This may be due to the poor thermal conductivity of TPU and the heat generated during the test cannot be released, which may influence the performance of each test. The testing point was easily burned out after measurements. The other problem was that the toluene in the ink solution has chemical reaction with TPU substrate, giving rise to the surface morphology change of TPU. The areas under different top electrodes may have variable performance. Several points changed from no properties to an unstable resistance change (X to X with yellow highlighted) was an evidence for the shape change of the substrate.

6. SUMMARY AND CONCLUSION

In this thesis, resistive switching devices based on CeO_2 nanomaterials have been fabricated and the electrical properties have been optimized through engineering the interface and point defects. CeO_2 thin films act as the switching media for the devices and they were prepared by solution processed methods via self-assembly of CeO_2 nanoparticles. The morphology and switching performances of thin films were improved by a UV/Ozone as well as plasma treatment. For the fabrication of the wearable devices, TPU, an elastic substrate, was used as stretchable substrates and the electrical properties in different stretching states were systematically studied.

First of all, pure and In-doped CeO_2 nanocrystals were synthesized using hydrothermal method. The CeO_2 nanocrystals were assembled into thin films for the fabrication of Au/ CeO_2 /Au/Si devices. It is interesting that doping process can improve the pack density [129] of the ink and help self-assembly thus ensure low cracking thin film with resistance change. Different percentage of doping would influence the self-assembly of the suspension ink, higher concentration of doping caused agglomeration affect the uniformity of the result thin film reduces the resistance change. Low concentration of doping would have a high on/off ratio for the thin film, vice versa. To balance the trade of memristor performance and rate of self-assembly of CeO_2 nanocrystals, i.e. achieving cracking-free state of CeO_2 thin film, a 5% doping of indium was chosen for the suspension ink.

Second, a thin film with a flat, non-cracking surface had more stable switching behaviors. The thin films were prepared by drop-coating and dried by a plasma treatment, which can activate more oxygen vacancy in nanocrystals. Herein, the role of oleic acid on the structure of the thin film has been studied. Oleic acid was an organic acid, which can increase the performance of self-assembly dramatically when adding in In-doped suspension ink. However, excess amount of oleic acid would increase the chance of agglomeration and conglomeration of the nanoparticle of the ink. On the other hand, organic acid with a high boiling point was hard to remove during drying or plasma treatment. Longer drying time was required for inks involved oleic acid. Overheating by plasma can cause crack generation and reduce the quality of the thin film. Herein, the solvent for suspension solution also affects the surface morphology of the film during drying process. It was found that toluene was more suitable than hexane as it had a higher boiling point. The final composition of the inks were chosen with a solvent of toluene at 5% In-doped followed by adding oleic acid afterwards (a ratio of ink : OLA is 1.5 : 1.)

Third, CeO_2 thin films with different layers were fabricated where very thick film had no resistance change, and very thin film resulted in cracking surface. Optimal resistive switching has been achieved in thin film device which has a relative small thickness and a flat cracking free surface. Some alternative surfactants were applied to improve the surface morphology of the thin film. Ligand calibration such as trioctylphosphine oxide (TOPO) can improve the crack generation of the film. However, TOPO was hard to dry and would leave an organic layer on top of the film, thus it was not applicable for the CeO_2 thin film

under the plasma treatment. Fourth, the role of top electrodes was also studied. For example silver top electrodes were successfully produced through ink-jet printing and the electrical properties were tested.

Finally, CeO_2 thin film flexible device was made using a TPU stretchable substrate. The device did not have perfect surface morphology due to the porous characteristic of the substrate. Resistive switching had been observed at a success rate of 30% from the sample device even after 100 'stretch-relax' cycles. Thus CeO_2 has potential for stretchable memory devices. More improvement could be done to improve the stability of resistance change of the device.

A success thin film device with a stretchable substrate can be involved in future flexible devices. Wearable devices with memristor characteristic would be one main future industry in the near future. A reduce of device size would be one critical requirement for the future device. This research on UV/ O_3 and plasma treatment can help improve the electrical characteristic of the switching materials and give rise to resistance change thus achieve a smaller size of the wearable device.

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